AT3 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1
PAG 13,14
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 13,14
DDRII 533,667 MHz

PCI-Express 16X

NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA
PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON
PAG 26

TV_OUT
CRT_OUT

CRT / S-VIDEO
PAG 25

LVDS(2 Channel)

Panel Connector
15" / 17" PAG 26

DMI LINK

NBSRCCLK, NBSRCCLK#

Cable Docking
PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

USB2.0
5 | 0,1,2 | 3 | 4,6,7

Bluetooth PAG 35
USB2.0 I/O Ports X3 PAG 32
Camera X1 PAG 32
Mini PCI-E Card x1
Express Card x1
Cable Docking x1

PCI BUS / 33MHz
PCI-E
Azalia

Option for 17" only
SATA - HDD PAG 35
SATA2

SATA - HDD PAG 32
SATA0 150MB

PATA- CD-ROM PAG 32
PATA (66/100/133)

SYSTEM CHARGER(MAX8724) PAG 41
SYSTEM POWER MAX8778 PAG 42
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 46
VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 43
VGACORE(1.025V)MAX1992 PAG 45
CPU CORE MAX8771 PAG 44

LPC

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

- Keyboard Touch Pad PAG 36
- CIR PAG 36
- Capacitive Sense SW PAG 36

X-Bus

- FAN PAG 38
- Flash PAG 37
- SPI PAG 37

Realtek
ALC 268
PAG 29

- Two-element microphone PAG 29
- Audio Jacks (Phone/ MIC) PAG 29

AUDIO Amplifier PAG 30
Jack to Speaker PAG 30

MDC DAA
SI3080
PAG 31
MODEM RJ 11 PAG 33

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 39

LAN
Realtek PCIE-LAN
RTL8101E/8111B
(10/100/GagaLAN
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 27,28

SIM CARD PAG 32
RJ45 PAG 33
IEEE1394 CONN PAG 28
Memory CardReader PAG 27

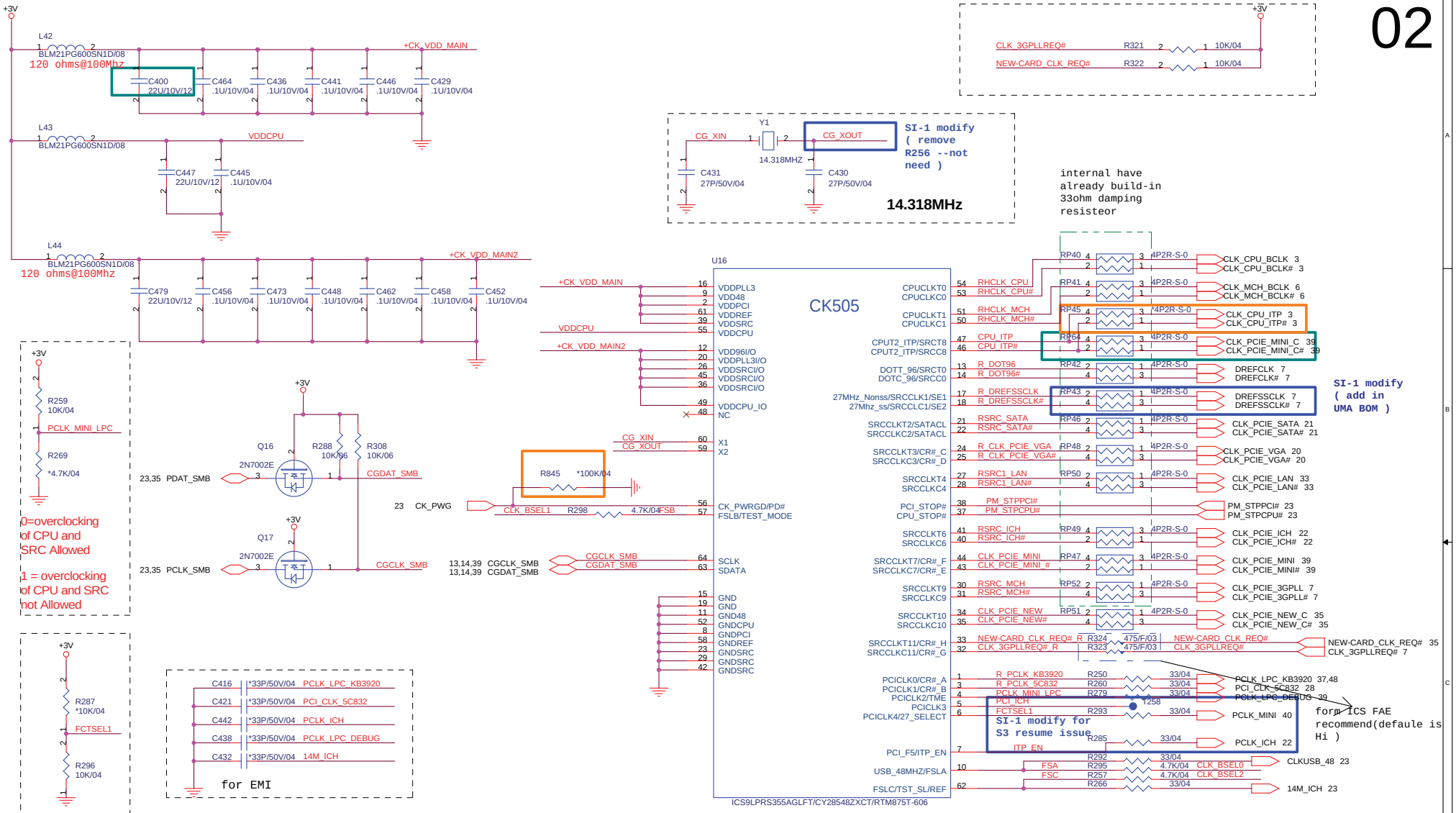
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Tuesday, January 09, 2007 Sheet 1 of 48



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

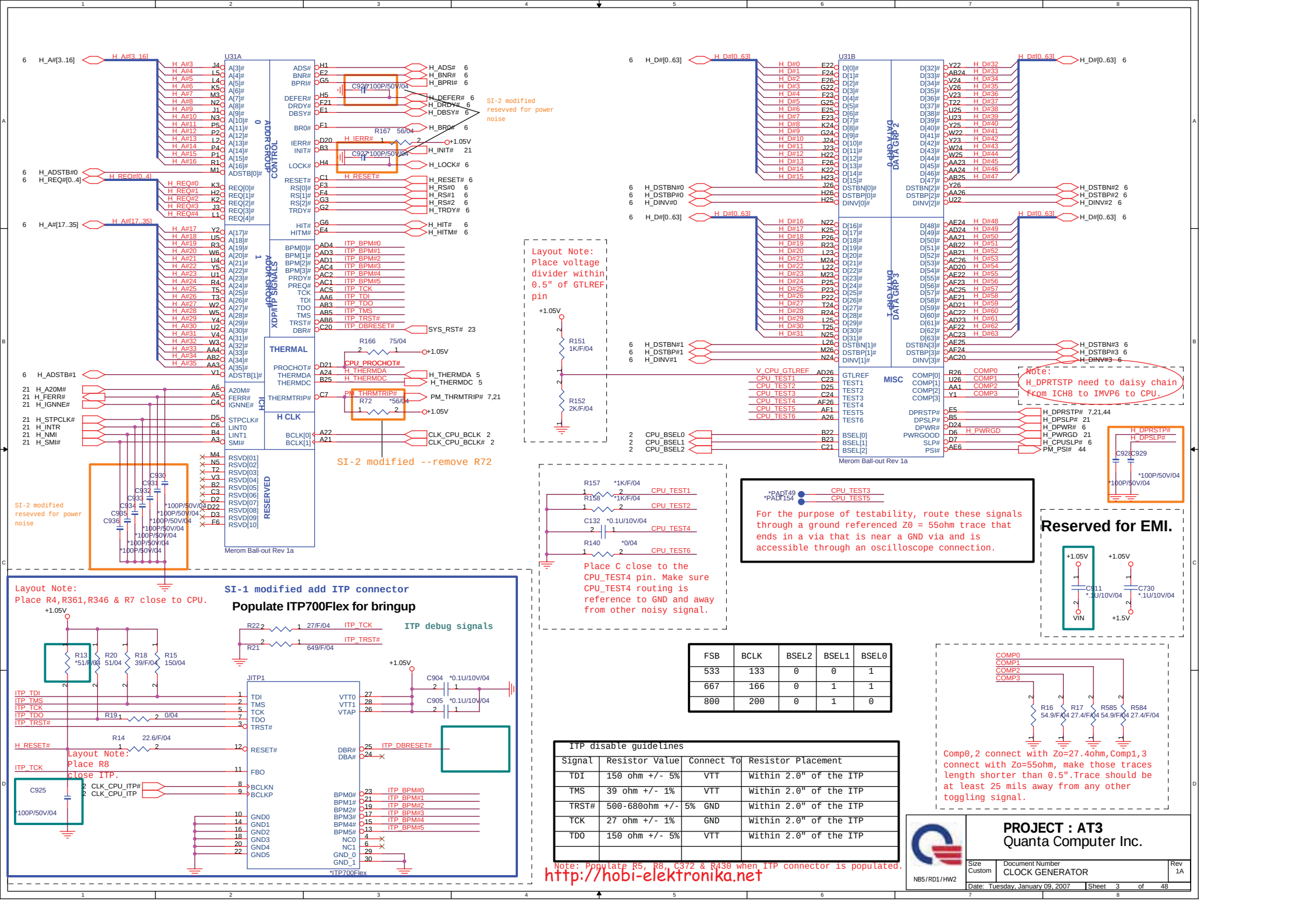
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

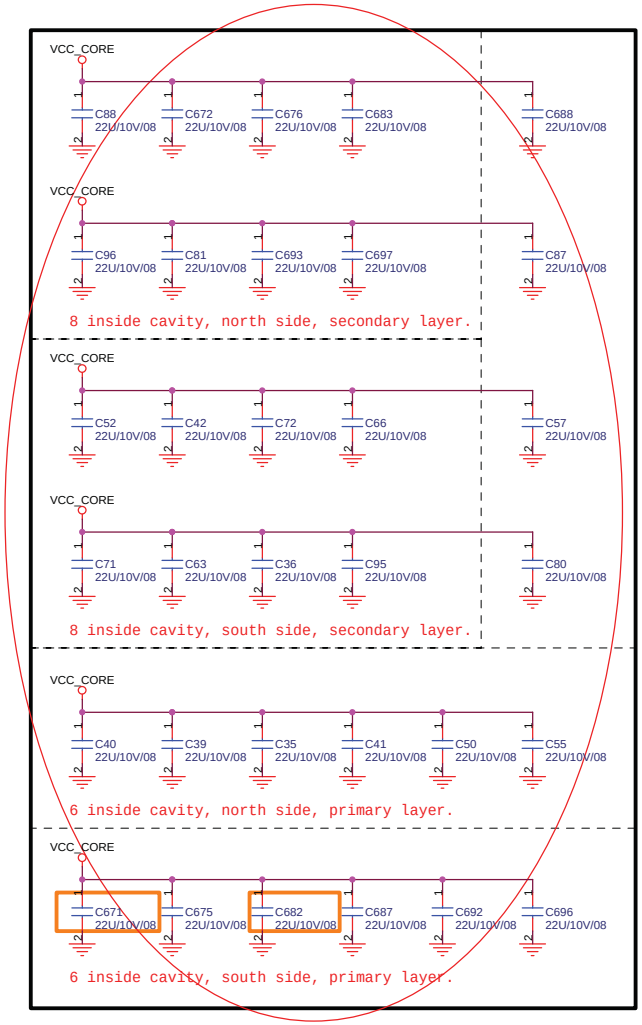
Date: Tuesday, January 09, 2007 Sheet 2 of 48

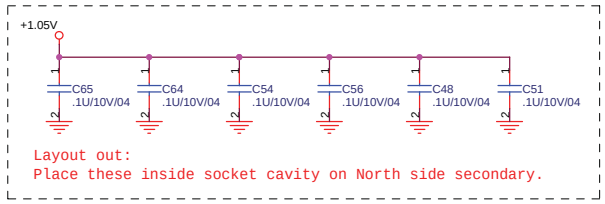


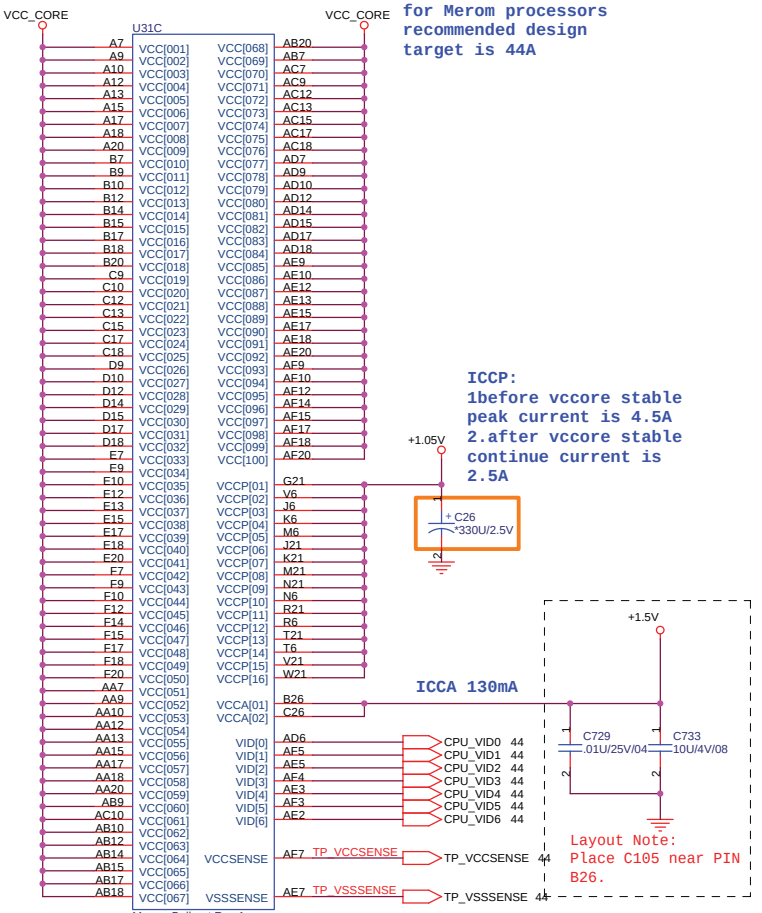
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

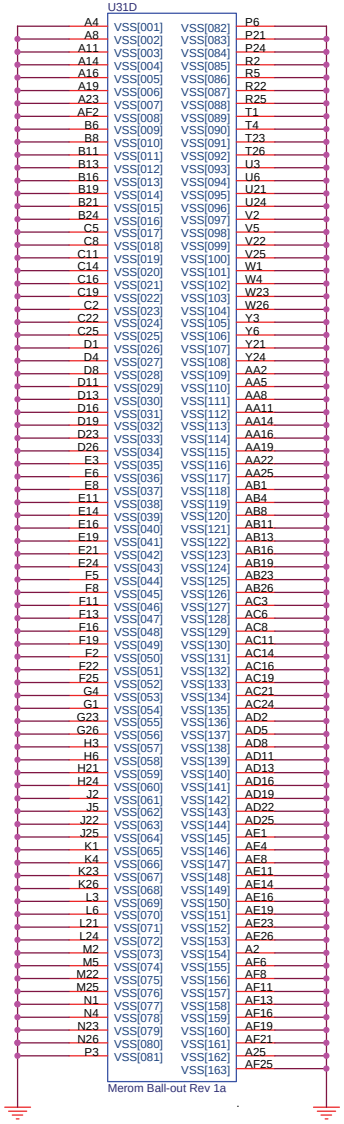
ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP



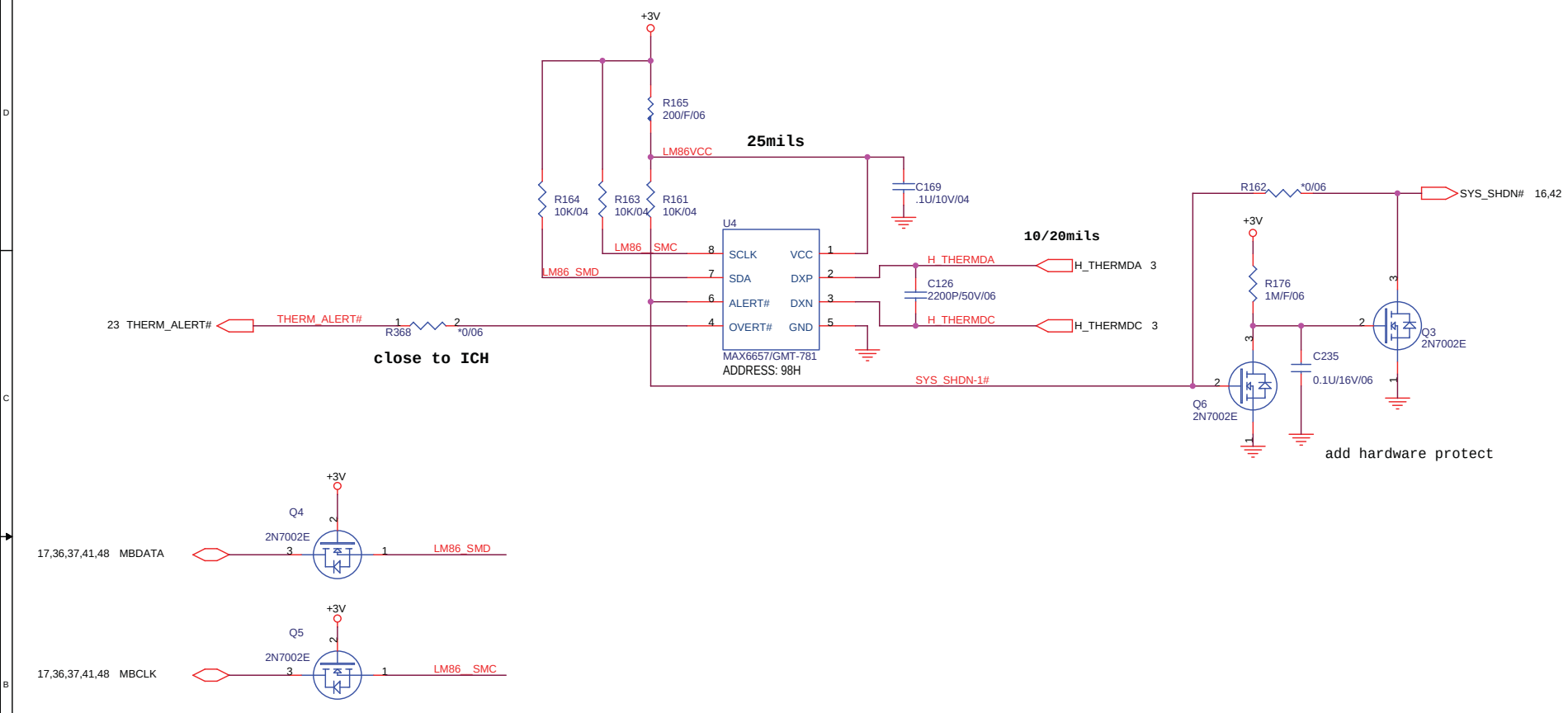






http://hobi-elektronika.net

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom — Document Number: Merom Processor (POWER)	Rev: 1A
	Date: Tuesday, January 09, 2007 — Sheet 4 of 48	

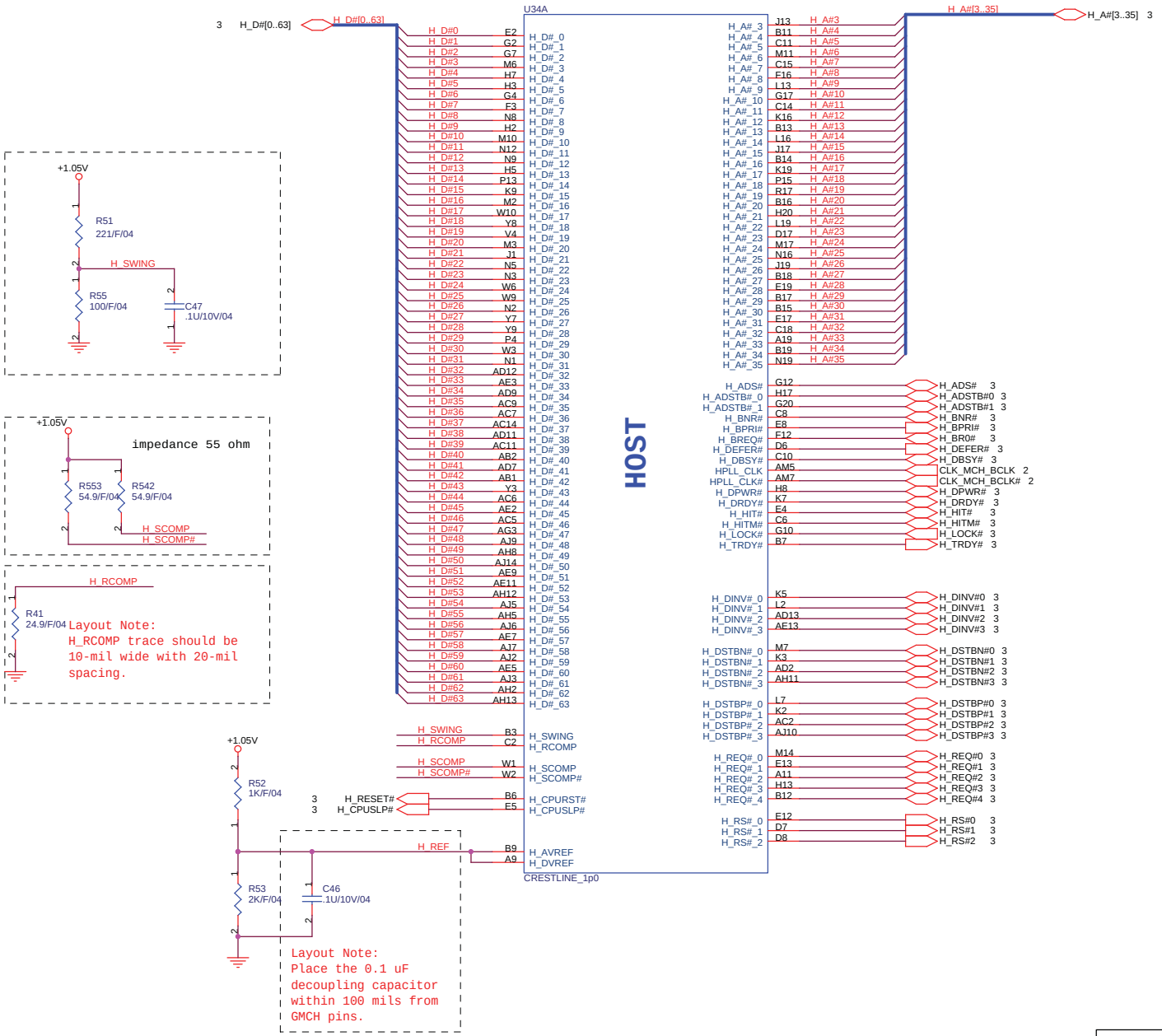


PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
B	THERMAL LM86	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 5 of 48

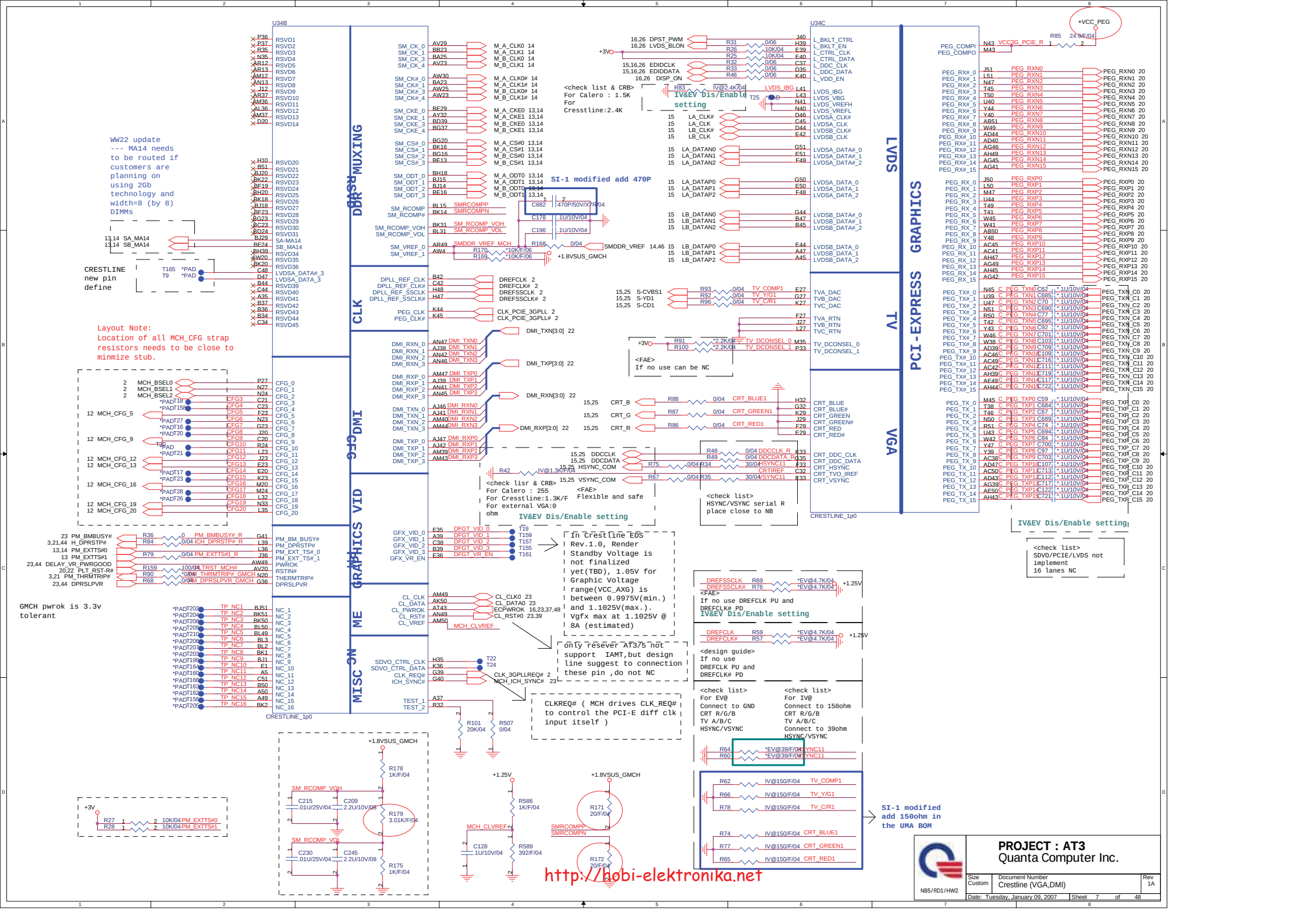


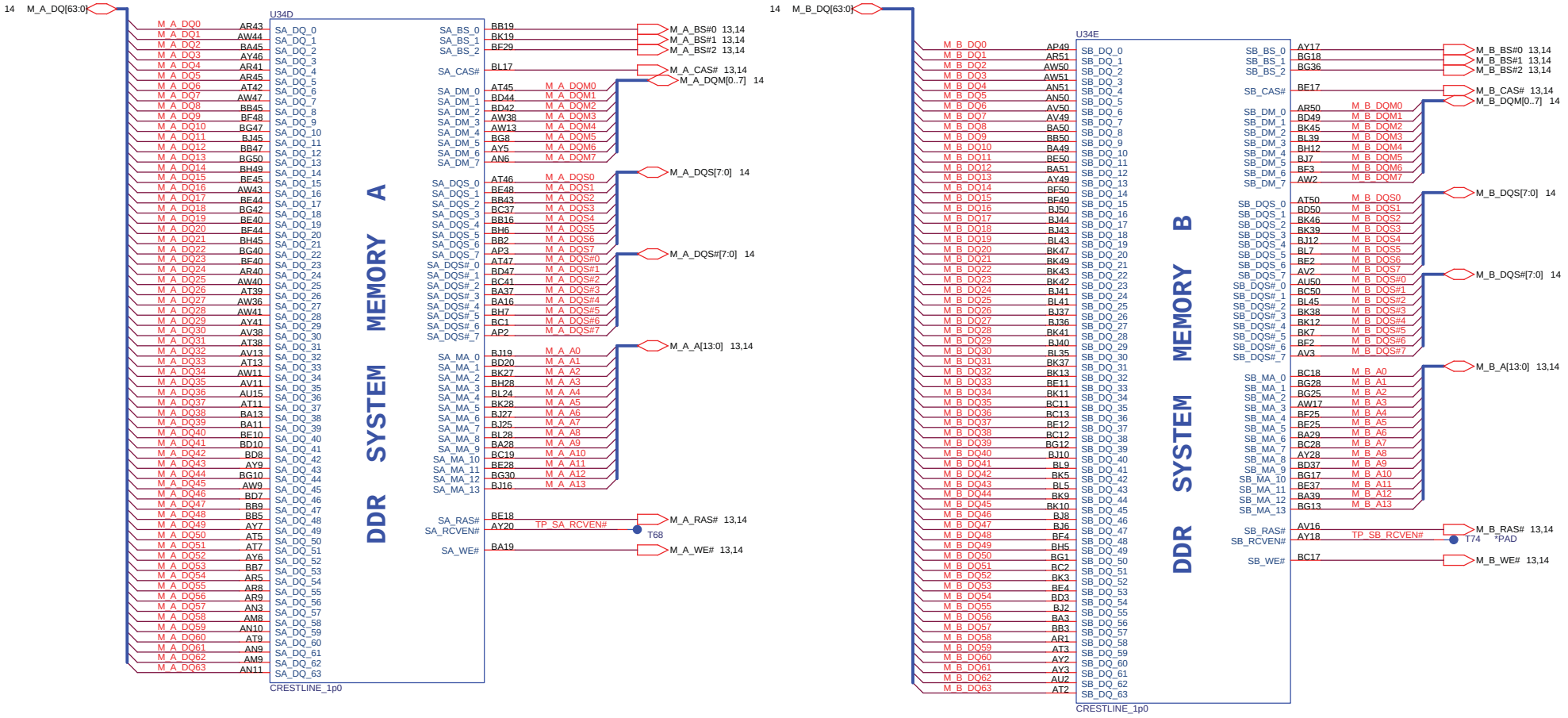
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (HOST)	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 6 of 48


U34B
U34C
DDR MUXING
CLK GEN
DMI
GRAPHICS VID
ME
MISC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CRESTLINE_1p0
WW22 update
--- MA14 needs
to be routed if
customers are
planning on
using 2Gb
technology and
width=8 (by 8)
DIMMs
CRESTLINE
new pin
define
Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minmize stub.
SI-1 modified add 470P
IV&EV Dis/Enable setting
<check list & CRB>
For Calero : 1.5K
For
Cresstline:2.4K
<FAE>
If no use can be NC
<check lisr & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0
ohm
<FAE>
Flexible and safe
<check list>
HSYNC/VSYNC serial R
place close to NB
In Crestline EDS
Rev.1.0, Render
Standby Voltage is
not finalized
yet(TBD), 1.05V for
Graphic Voltage
range(VCC_AXG) is
between 0.9975V(min.)
and 1.1025V(max.).
Vgfx max at 1.1025V @
8A (estimated)
only reserver AT3/5 not
support IAMT,but design
line suggest to connection
these pin ,do not NC
CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)
<check list>
SDVO/PCIE/LVDS not
implement
16 lanes NC
<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC
<check list>
For IV@
Connect to 150ohm
CRT R/G/B
TV A/B/C
Connect to 39ohm
HSYNC/VSYNC
<design guide>
If no use
DREFCLK PU and
DREFCLK# PD
<FAE>
If no use DREFCLK PU and
DREFCLK# PD
SI-1 modified
add 150ohm in
the UMA BOM
GMCH pwrok is 3.3v
tolerant
+VCC_PEG
+1.8VSUS_GMCH
+1.25V
+3V
PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number Crestline (VGA,DMI)
Rev 1A
Date: Tuesday, January 09, 2007
Sheet 7 of 48
http://hobi-elektronika.net



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	1A

Date: Tuesday, January 09, 2007 Sheet 8 of 48

POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

SI-1 modify (remove R73,R11 --not need)

SI-2 modified --remove C91&C108

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

for IAMT power if not support need to connection to S0 power

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

Layout Note: Place close to GMCH edge.

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

CRESTLINE_1p0

CRESTLINE_1p0

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VCC, NCTF)	1A

Date: Tuesday, January 09, 2007 Sheet 9 of 48

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

SI-1 modify
(NET name
wrong)

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

50mA
150mA
80mA
80mA
10uH+-20%_100mA

0.1Caps should be
placed 200 mils
with in its pins.

IV&EV Dis/Enable setting

10mA

Ivcca_PEG_BG
supply current
100mA

100mA

POWER

CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
D TV/CRT
LVDS

VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF

CRESTLINE_1p0

Ivcc_VTT FSB
supply
current
0.85A

Place on the edge.

Place on the edge.

Reserved L81 pad for
inductor.

Place caps close
to VCC_AXD.

Ivcc_DMI supply
current 100mA

200mA

100mA

1uH+-20%_300mA

IV&EV Dis/Enable setting

Ivcc_PEG
supply current
1.2A

SI-1 modified change

Ivcc_RX_DMI
supply current
250mA

+3V_VCC_HV

40 mil
wide

Place caps close
to VCC_AXF

SI-2
modified
for WW48
request

SI-2 add for UMA to
fix TV-out noise

FB_180ohm+-25%
100mHz_1500mA_
0.09ohm DC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

250mA

150mA

22nF & 0.1uF for
VCC_TVDACA:C_R should
be placed with in 250
mils from Crestline.

IV&EV Dis/Enable setting

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

100mA

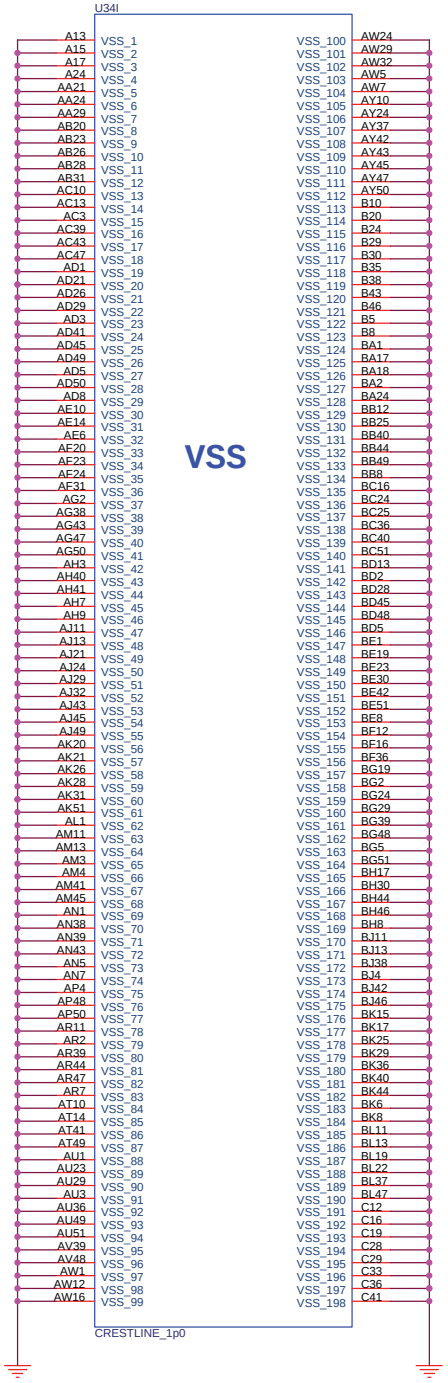
1uH+-20%_300mA

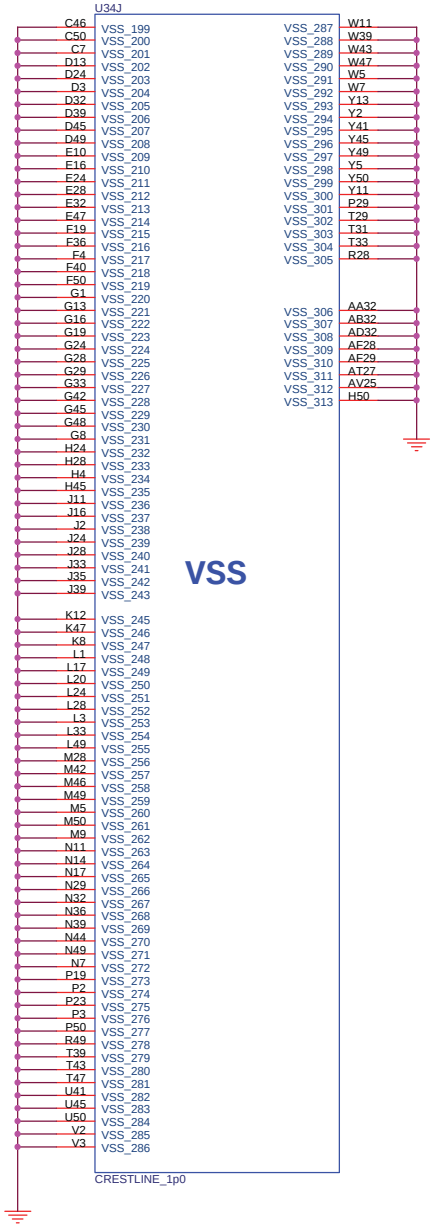
PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size: Custom | Document Number: Crestline (POWER) | Rev: 1A

Date: Tuesday, January 09, 2007 | Sheet 10 of 48





NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VSS)	1A

Date: Tuesday, January 09, 2007 Sheet 11 of 48

Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

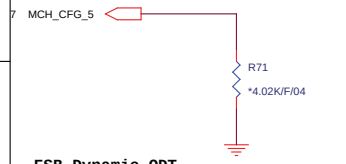
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

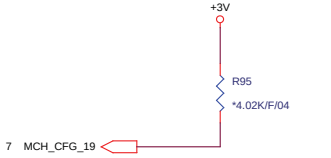
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

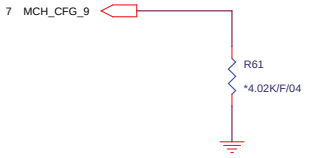


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

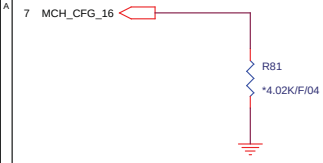


SDVO Present

Strap define at External DVI control page

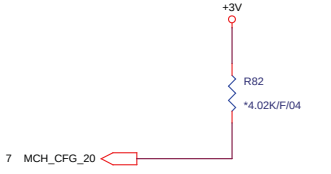
FSB Dynamic ODT

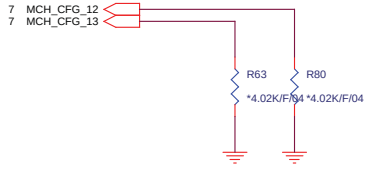
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

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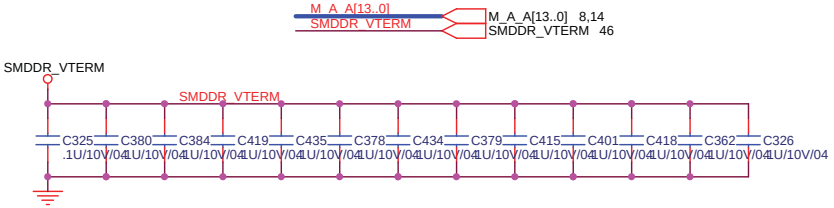
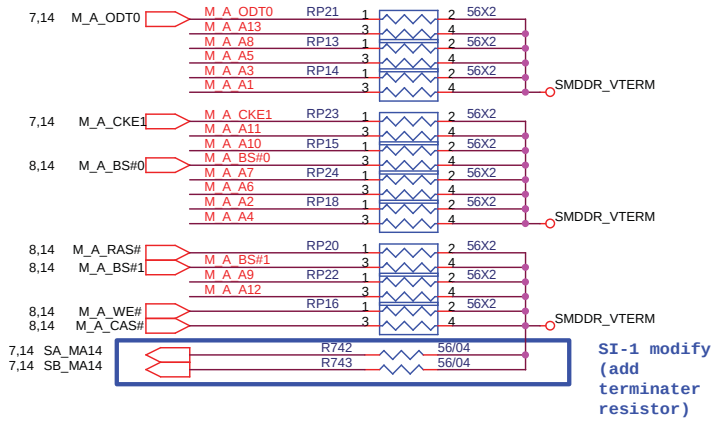
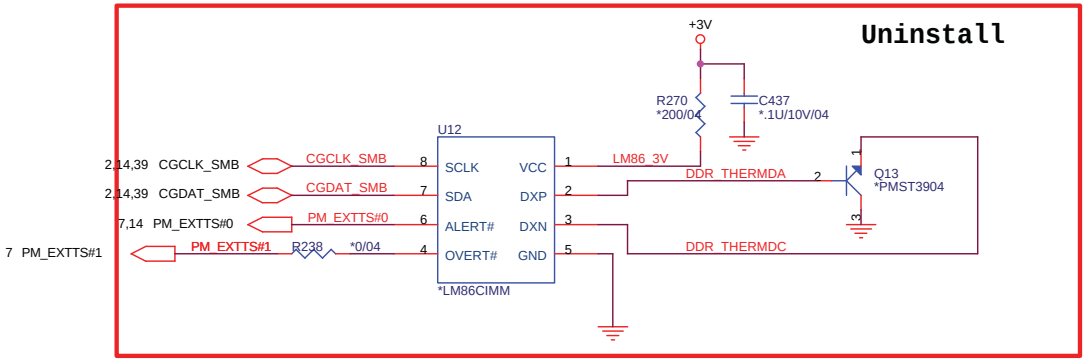
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

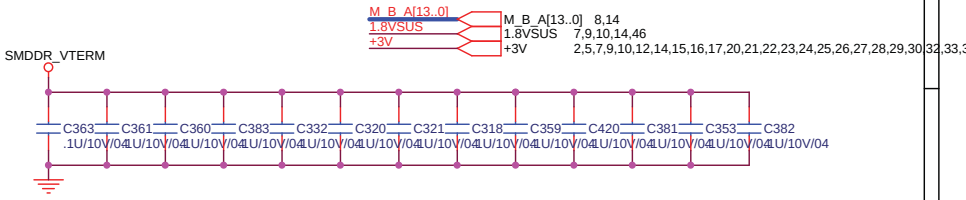




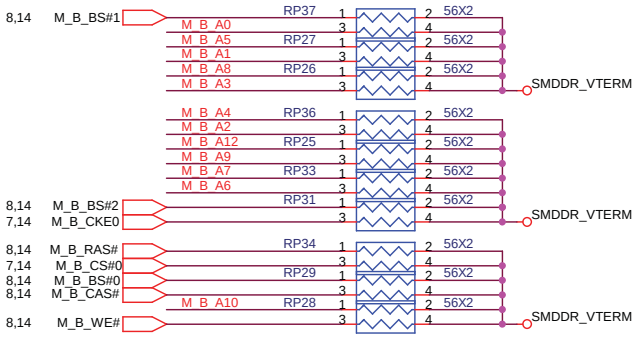
SI-1 modify (add terminater resistor)

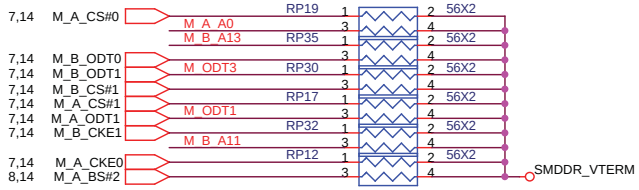


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





PROJECT : AT3 Quanta Computer Inc.		
Size: B	Document Number: DDRII RES.ARRAY	Rev: 1A
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NB5/RD1/HW2

CGCLK_SMB
CGDAT_SMB
CGCLK_SMB 2,13,39
CGDAT_SMB 2,13,39

M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_CKE[0..1] 7,13
M_A_CS#[0..1] 7,13

M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_RAS# 8,13
M_A_CAS# 8,13
M_A_WE# 8,13

M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_CLK0 7
M_A_CLK0# 7
M_A_CLK1 7
M_A_CLK1# 7
M_A_BS#[0..2] 8,13
M_A_ODT[0..1] 7,13

M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]
M_A_DQM[0..7] 8
M_A_DQ[0..63] 8
M_A_DQS[0..7] 8
M_A_DQS#[0..7] 8
M_A_A[13..0] 8,13

M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_CKE[0..1] 7,13
M_B_CS#[0..1] 7,13

M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_RAS# 8,13
M_B_CAS# 8,13
M_B_WE# 8,13

+3V
1.8VSUS
+3V 2,5,7,9,10,12,13,15,16,17,20,21,22,23,24,25,26,27,28,29,30,32,33,35,36,37,38,39,40,42,47
1.8VSUS 7,9,10,46

M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_CLK0 7
M_B_CLK0# 7
M_B_CLK1 7
M_B_CLK1# 7
M_B_BS#[0..2] 8,13
M_B_ODT[0..1] 7,13

M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]
M_B_DQM[0..7] 8
M_B_DQ[0..63] 8
M_B_DQS[0..7] 8
M_B_DQS#[0..7] 8
M_B_A[13..0] 8,13

PC2100 DDR2 SDRAM SO-DIMM (200P)

M_B_DQ[0..63] M_B_A[0..13] M_B_BS#[0..2] M_B_CKE[0..1] M_B_CS#[0..1] M_B_RAS# M_B_CAS# M_B_WE# M_B_ODT[0..1] M_B_DQM[0..7] M_B_DQS[0..7] M_B_DQS#[0..7] M_B_CLK0 M_B_CLK0# M_B_CLK1 M_B_CLK1# CGCLK_SMB CGDAT_SMB DIM2_SA0 DIM2_SA1 +3V

CKEA 0,1
H 9.2

FOX=AS0A426-M2S-TR
CN26A

PC2100 DDR2 SDRAM SO-DIMM (200P)

M_A_DQ[0..63] M_A_A[0..13] M_A_BS#[0..2] M_A_CKE[0..1] M_A_CS#[0..1] M_A_RAS# M_A_CAS# M_A_WE# M_A_ODT[0..1] M_A_DQM[0..7] M_A_DQS[0..7] M_A_DQS#[0..7] M_A_CLK0 M_A_CLK0# M_A_CLK1 M_A_CLK1# CGCLK_SMB CGDAT_SMB DIM1_SA0 DIM1_SA1 +3V

CKEB 0,1
H 5.2

FOX=AS0A426-MAS-TR
CN24A

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM
7,13 PM_EXTTS#0
SI-1 CHANGE
7,13 SB_MA14
M_B_A13
M_B_ODT0
M_B_ODT1

FOX=AS0A426-M2S-TR
CN26B

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM
7,13 PM_EXTTS#0
SI-1 CHANGE
7,13 SA_MA14
M_A_A13
M_A_ODT0
M_A_ODT1

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
SMDDR_VREF_DIMM
R226 0/06
SMDDR_VREF 7,46
R227
1.8VSUS
R603 *10K/F/06
*10K/F/06

DIM2_SA0 R267 10K/04
DIM2_SA1 R268 10K/04
+3V
SMbus address A4

R216 10K/04 DIM1_SA0
R217 10K/04 DIM1_SA1
SMbus address A0

Place these Caps near So-Dimm1.

1.8VSUS
C773 2.2U/6.3V/06
C775 2.2U/6.3V/06
C785 2.2U/6.3V/06
C444 2.2U/6.3V/06
C764 2.2U/6.3V/06
C770 .1U/10V/04
C788 .1U/10V/04
C439 .1U/10V/04
C433 .1U/10V/04
C769 .1U/10V/04
C767 .1U/10V/04

SMDDR_VREF_DIMM
C772 .1U/10V/04
C768 2.2U/6.3V/06

+3V
C317 2.2U/6.3V/06
C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS
C774 2.2U/6.3V/06
C786 2.2U/6.3V/06
C784 2.2U/6.3V/06
C759 2.2U/6.3V/06
C760 .1U/10V/04
C776 .1U/10V/04
C789 .1U/10V/04
C787 .1U/10V/04
C443 .1U/10V/04
C765 .1U/10V/04
C766 .1U/10V/04

SMDDR_VREF_DIMM
C371 .1U/10V/04
C373 2.2U/6.3V/06

+3V
C372 2.2U/6.3V/06
C385 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	1A
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YELLOW BLOCK is for G8X chip only

SI-1 modify (change from bead to 0 ohm)

need add to 3v

YELLOW BLOCK is for G8X chip only

FOR G72M/G73M only

OPTION SIGNAL FROM NB FOR UMA VGA

OPTION SIGNAL FROM Nvidia to VGA

C34: PUN issue reserve
U54,C950,c949,R726,R727

Vout=1.25(1+Ra/Rb)

FOR IFPC VDD LEAKAGE CIRCIUT

SPREAD SPECTRUM

I2C ADDRESS: 0xD4H

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size: Custom | Document Number: NVG73M (LVDS/DVI/CRT/TV) | Rev: 1A

Date: Tuesday, January 09, 2007 | Sheet 15 of 48

ROM_TYPE(0:1) resister can be remove due to from nvidia HANK recommend need to reserve or cancel

PCI_DEVICE[3:0] Default are "0",can remove pull down resister from nvidia HANK recommend

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

GREEN BLOCK can remove if use G8X

MIOBD7 pull down and MIOB_DE pull up from nvidia HANK recommend

SHARE M/B SYSTEM BIOS, SUB VENDOR ID NEED PULL DOWN .

SI-2 ADD for Nvidia requests

SI-2 MODIFIED

YELLOW BLOCK is for G8X chip only

GFX_VID0
H : Low Voltage
L : Normal Voltage

VGACORECTL	G73M
HI	1.0V
LO	1.1V

SI-1 MOVE DISP_ON

SI-1 MOVE LVDS_BLON

GPIO1 PULL DOWN strap can be remove from nvidia HANK recommend

G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

GREEN BLOCK can remove if use G8X

GPIO12	G8X
HI	AC MODE
LO	BAT MODE

SI-2 MODIFIED

FOR BATTERY MODE throttling FUNCTION

VGA THERMAIL CIRCUIT

Default are "0",can remove pull down resister from nvidia HANK recommend

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	NVG73M (ROM/GPIO/STRAP)	1A

Date: Tuesday, January 09, 2007 Sheet 16 of 48

Channel C is available on G73M only

U37B

U37C

FBA

FBC

*U_GPU_G3

PLACE NEAR GPU

PLACE NEAR GPU

C783 *220U

GREEN BLOCK can remove if use G8X

YELLOW BLOCK is for G8X chip only

YELLOW BLOCK is for G8X chip only

15mil

G72: Stuff these parts
G73M : NC

For EMI

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

G72M/G73M: STUFF
UMA:NC

G72M/G73M: STUFF
UMA:NC

F_VREF2 filter can be remove from nvidia HANK recommend
G70,G71: Stuff these parts
G72M,G73M : NC

SI-2 modified for G8X thermal sensor

http://hobi-elektronika.net

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (MEM I/F)	1A

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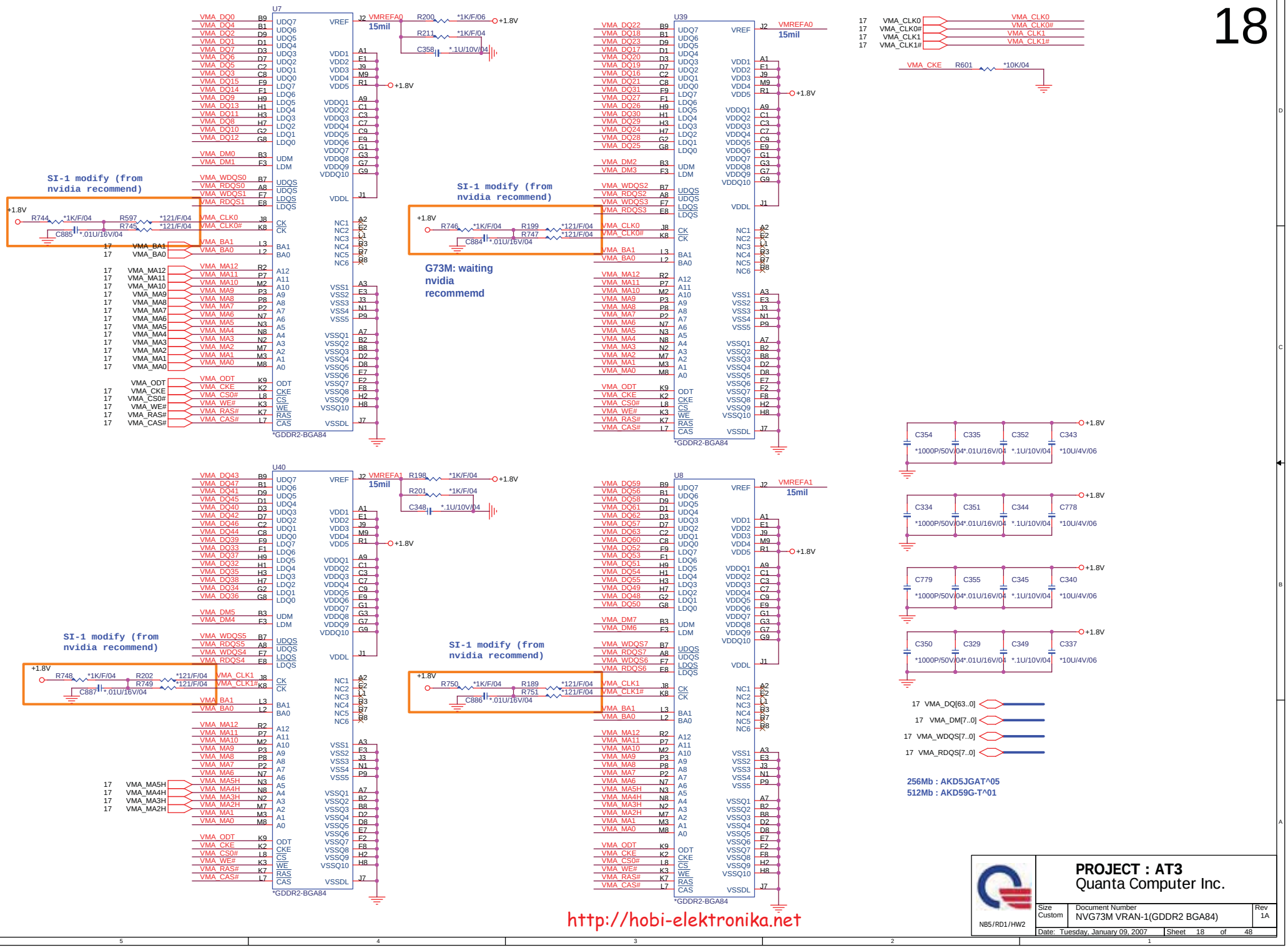
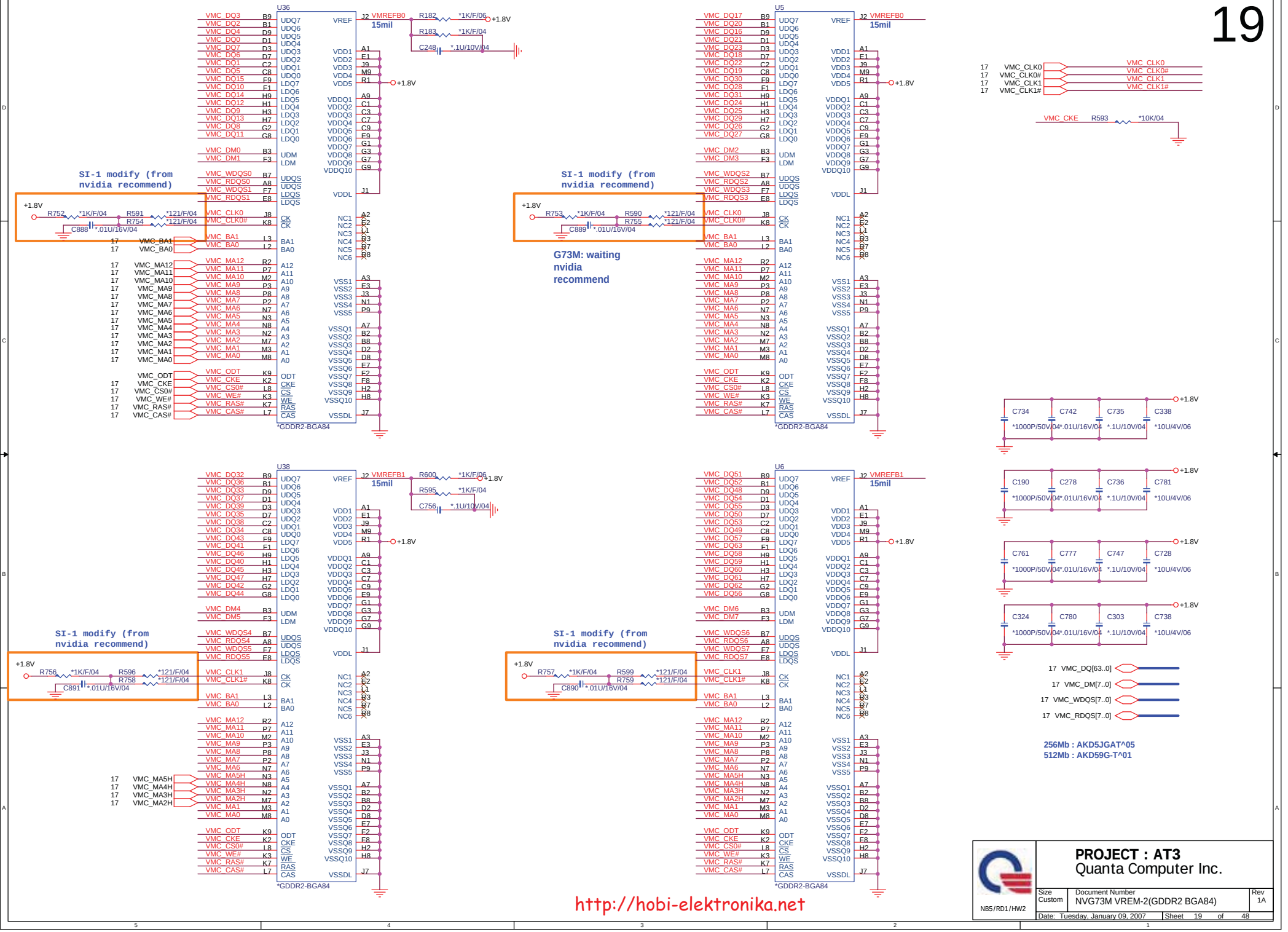
NB5/RD1/HW2





PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: NVG73M VREM-2(GDDR2 BGA84)
Rev: 1A	
Date: Tuesday, January 09, 2007	Sheet 19 of 48

U37F

*U_GPU_G3

U37A

PCIE

*U_GPU_G3

500mA

45,47 VGACORE → VGACORE

15,17,46,47 VGA1.2V → VGA1.2V

VGA1.2V

PLACE NEAR GPU

1500mA

VGACORE

PLACE NEAR GPU

G8X Total power consumption
1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
2.PCIE VGA1.2V -- 1.75A
3.FBVDDQ 1.8V ----- 3.12A
4.VDD I/O 3.3V ---- 0.49A
5.PLL 2.5V ---

power up sequence

I/O 3.3V
NVCORE
1.8VFBDDQ
1.2V
2.5V

PLACE NEAR GPU

180mA

20mA

15mil

SI-1 modify (change part number)

SI-2 modify for Nvidia requests
del R823,R824

For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.

+3V

D3 *CH501H-40PT L-F

D2 *CH501H-40PT L-F

R114 *24.3K/F/04

R106 *3.4K/F/06

R123 *76.8/F/04

SPDIF_VGA C943 *.01U/16V/04 SPDIF 29,38

U3 *TC7SH08FU

C98 *1U/6.3V/06

R138 *100/04

R139 *0/04

R587 *10K/04

7,22 PLT_RST-R#

PLT_RST-R#

VGA_RST#

T82 VGA_RFU0 AG12 RFU0

T80 VGA_RFU1 AH13 RFU1

T200 PEX_TSTCK AM12 PEX_TSTCLK_OUT

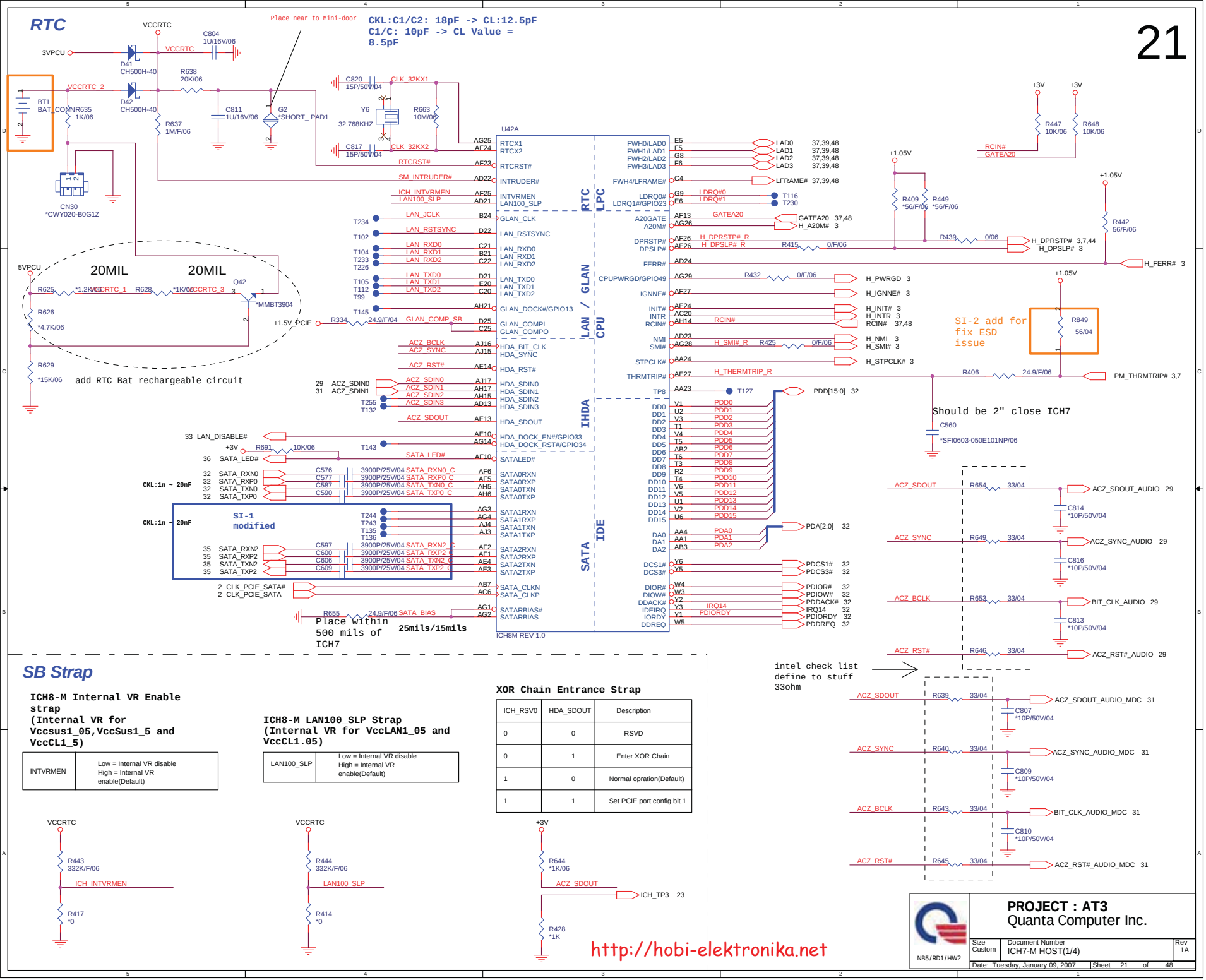
T197 PEX_TSTCK# AM11 PEX_TSTCLK_OUT#

SPDIF J6 SPDIF_VGA

T84 VDD_SENSE

T85 GND_SENSE

PROJECT : AT3	Quanta Computer Inc.
NB5/RD1/HW2	Size: Custom; Document Number: NVG73M (PCIE I/F); Rev: 1A
	Date: Tuesday, January 09, 2007; Sheet 20 of 48



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

PROJECT : AT3 Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: ICH7-M HOST(1/4)	Rev: 1A
	Date: Tuesday, January 09, 2007	Sheet 21 of 48

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E

SI-2 Add for support RBSON card

PCIE-LAN

U42D

PCI-Express Direct Media Interface

SPI

USB

ICH8M REV 1.0

15/15mils

Place within 500 mils of ICH7

R379 24.9/F/06

+1.5V

USB Connector

USB Connector

FINGERPRINT

Carama USB

Docking

BLUETOOTH

WWAN

NEW CARD

USB Connector

SI-2-1 swaped for fix dash issue

USB Connector

SI-1 modified from HP request

25mils/15mils

Place within 500 mils of ICH8

R632 22.6/F/06

RP61 8.2KX8

RP62 8.2KX8

RP63 8.2KX8

RP53 10P8R-10K

CHECK LIST suggest pull up 10k

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K

U42B

PCI

Interrupt I/F

ICH8M REV 1.0

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

U41 TC7SH08FU

C792 0.1U/16V/06

Don't connect to PCI device / Express card

for EMI request

PCLK_ICH R328 *0 C484 *33P/50V

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size: Custom | Document Number: ICH7-M M PCI E(2/4) | Rev: 1A

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SI-2 Add for fix re-boot fail

R833 2K/F/04

U26 NL17SZ14DFT2G

C608 .1U/16V/04

44 VR_PWRGD_CK410#

VR_PWRGD_CK410

R809 100K/04

SI-1 has modified it ,please measure BOM has add(intel checklist add)

SI-1 add

PCLK_SMB R617 2.2K/06
PDAT_SMB R272 2.2K/06
PCIE_WAKE# R399 1K/06
PM_BATLOW# R R387 8.2K/06

SMB_LINK_ALERT# R621 10K/06
SMLINK0 R619 10K/06
SMLINK1 R618 10K/06

RI# R624 8.2K/06
DNBSWON# R271 10K/06
SYS_RST#-1 R615 10K/06
SMB_ALERT# R273 10K/06

KBSMI# R R281 10K/06

SI-1 modified

SWI# R R280 10K/06

CLKRUN# R433 8.2K/06
SERIRQ R656 8.2K/06
SCI# R R662 10K/06

PM_RSMRST# R R658 10K/06

these pin if unused require 8.2k to 10k pull-up to +3V

U42C ICH8M REV 1.0

SMBCLK SMBDATA LINKALERT# SMLINK0 SMLINK1 — SMB

RI# — SYS GPIO

SUS_STAT#/LPCPD# SYS_RESET# BMBUSY#/GPIO0 SMBALERT#/GPIO11 STP_PCI#/GPIO15 STP_CPU#/GPIO25 CLKRUN#/GPIO32 WAKE# SERIRQ THRM# VRMPWRGD TP7 — Power MGT

TACH1/GPIO1 TACH2/GPIO6 TACH3/GPIO7 GPIO8 GPIO12 TACH0/GPIO17 GPIO18 GPIO20 SCLOCK/GPIO22 QRT_STATE0/GPIO27 QRT_STATE1/GPIO28 SATACLKREQ#/GPIO35 SLOAD/GPIO38 SDATAOUT0/GPIO39 SDATAOUT1/GPIO48 — GPIO

SPKR MCH_SYNC# TP3 — MISC

SATA0GP/GPIO21 SATA1GP/GPIO19 SATA2GP/GPIO36 SATA3GP/GPIO37 — SATA GPIO

BOARD_ID1 BOARD_ID0 BOARD_ID3 BOARD_ID4

CLK14 CLK48 SUSCLK — Clocks

14M_ICH CLKUSB_48

SLP_S3# SLP_S4# SLP_S5# BATLOW# PWRBTN# LAN_RST# RSMRST# CK_PWRGD CLPWROK SLP_M# — Power MGT

CL_CLK0 CL_CLK1 CL_DATA0 CL_DATA1 CL_VREF0 CL_VREF1 CL_RST# — Controller Link

MEM_LED/GPIO24 ME_EC_ALERT/GPIO10 EC_ME_ALERT/GPIO14 WOL_EN/GPIO9

R450 *10K/F/06 R315 *10K/F/06 SYS_RST#

R682 0/04 PM_BMBUSY#

R402 0/F/06 R436 0/F/06 PM_STPPCI_ICH# PM_STPCPU_ICH#

2 PM_STPPCI# 2 PM_STPCPU#

28,37,48 CLKRUN#

33,35,39 PCIE_WAKE# 28,37,40,48 SERIRQ

5 THERM_ALERT# R364 8.2K/06

T245 T254

37 KBSMI# 37 SCI# 37 SWI#

R405 0/04 KBSMI# R
R386 0/04 SCI# R
R611 0/04 SWI# R

30 AMPBEEP_EN 26 LCD_BK

LCD_BK BOARD_ID2

39 WAN_OFF# 39 RF_OFF# 36 BTLED

R687 0/04 R671 0/04 R420 0

R768 10K/04 R769 10K/04 R770 10K/04

SI-1 add

30 ACZ_SPKR

7 MCH_ICH_SYNC# R427 0 R435 *10K

MCH_ICH_SYNC# R

21 ICH_TP3

SATA0GP/GPIO21 AJ12 BOARD_ID1
SATA1GP/GPIO19 AJ10 BOARD_ID0
SATA2GP/GPIO36 AF11 BOARD_ID3
SATA3GP/GPIO37 AG11 BOARD_ID4

CLK14 AG9 14M_ICH 2
CLK48 G5 CLKUSB_48 2

SUSCLK D3 T108

SLP_S3# AG23 R616 100/F/06 SUSB# 37,48
SLP_S4# AF21 R326 100/F/06 SUSC# 37,48
SLP_S5# AD18 T130

S4_STATE#/GPIO26 AH27 T249

PWROK AE23 ICH_PWROK R677 *100K/04

DPRSLPVR/GPIO16 AJ14 DPRSLPVR-ICH R620 499/F DPRSLPVR DPRSLPVR 7,44

BATLOW# AF21 PM_BATLOW# R R642 0/04 PM_BATLOW# 37
DNBSWON# DNBSWON# 37

PWRBTN# C2 C819 *.1U/16V/04 R665 *100/F/06

LAN_RST# AH20 PLTRST_LAN# R666 100/F/06 LAN_REST 33,37,48 PLTRST# 22,32,33,35,37,39

RSMRST# AG27 PM_RSMRST# R R659 100/F/06 RSMRST# RSMRST# 37,48

CK_PWRGD E1 R623 0/04 CK_PWG 2

CLPWROK E3 R622 0/04 ECPWROK 7,16,37,48

SLP_M# AJ25 SUSM# T251

CL_CLK0 F23 CL_CLK0 7
CL_CLK1 AE18 ICH_CL_CLK1 39

CL_DATA0 F22 CL_DATA0 7
CL_DATA1 AF19 ICH_CL_DATA1 39

CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB

CL_RST# AJ23 CL_RST#0 7,39

MEM_LED/GPIO24 AJ27 R284 0/04 BT_OFF# 35
ME_EC_ALERT/GPIO10 AJ24 ME_SMC_ALERT# T250
EC_ME_ALERT/GPIO14 AF22 T141
WOL_EN/GPIO9 AG19 T144

SI-2 change from 100ohm to 499 ohm check list -- series 500ohm to IMVP6+

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#

3V_S5 R631 3.24K/F/06 R633 453/F/04 C798 .1U/10V/04

Controller Link 1 VREF for IAMT support only

+3V R338 3.24K/F/06 R344 453/F/04 C511 .1U/10V/04

Controller Link 0 VREF for IAMT support only

R819 10K/04 3VSUS

SI-1 ADD (ww36 request)

CRB STUFF 2K%1 R657 2K/F/04

3VSUS C818 .047U/10V/04

7,44 DELAY_VR_PWRGOOD
7,16,37,48 ECPWROK

U43 TC7SH08FU

R661 100K/06 R667 10K/06 ICH_PWROK

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

ACZ_SPKR R411 *10K

SI-2 Change

R660 *10K/06 BOARD_ID3 R760 10K/06
R652 *10K/06 BOARD_ID4 R761 10K/06
R692 *10K/06 BOARD_ID0 R693 10K/06
R688 *10K/06 BOARD_ID1 R448 10K/06
R690 *10K/06 BOARD_ID2 R689 10K/06

SI-1 modify (for board ID select)

Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15"PAV Discrete 965PM+G86MV+128M (0:1:0)	17" PAV Discrete 965PM+G86MV+128M (0:1:1)	17" PAV Discrete 965PM+G84MV+256M (1:0:0)	17" PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size: Custom | Document Number: ICH7-M GPIO(3/4) | Rev: 1A

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1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

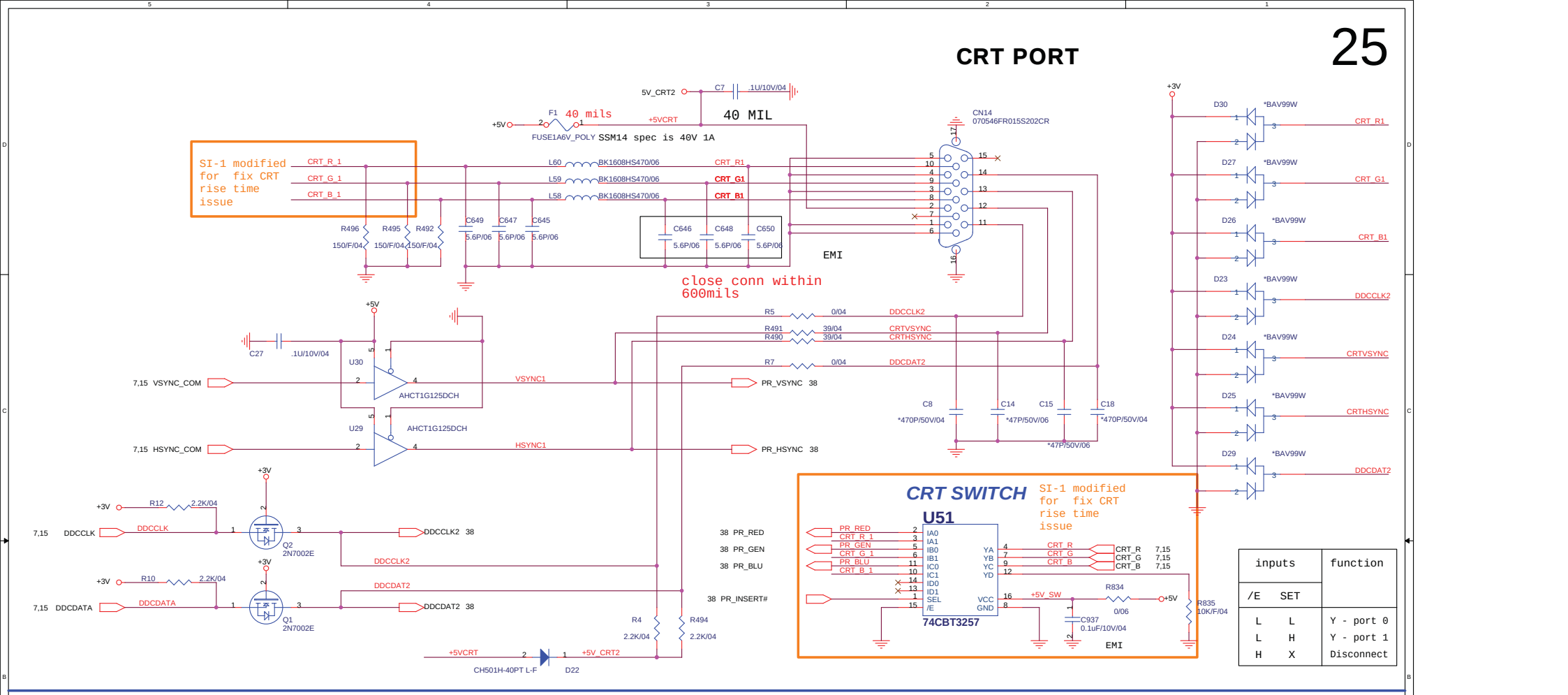
V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
SI-2 modified (remove R374)
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

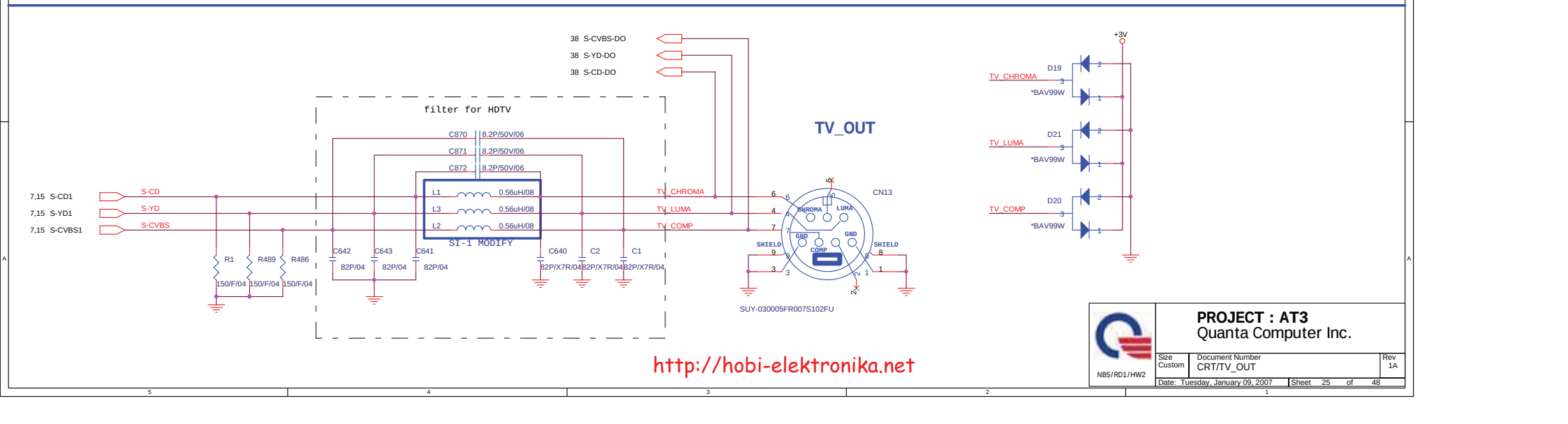
Can be connect to +3V_S5 or 1.5V_S5
Can be connect to +3V or +1.5V

U42E — ICH8M REV 1.0
U42F — ICH8M REV 1.0

PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: ICH7-M POWER(4/4)
Rev: 1A	
Date: Tuesday, January 09, 2007	Sheet 24 of 48

CRT PORT





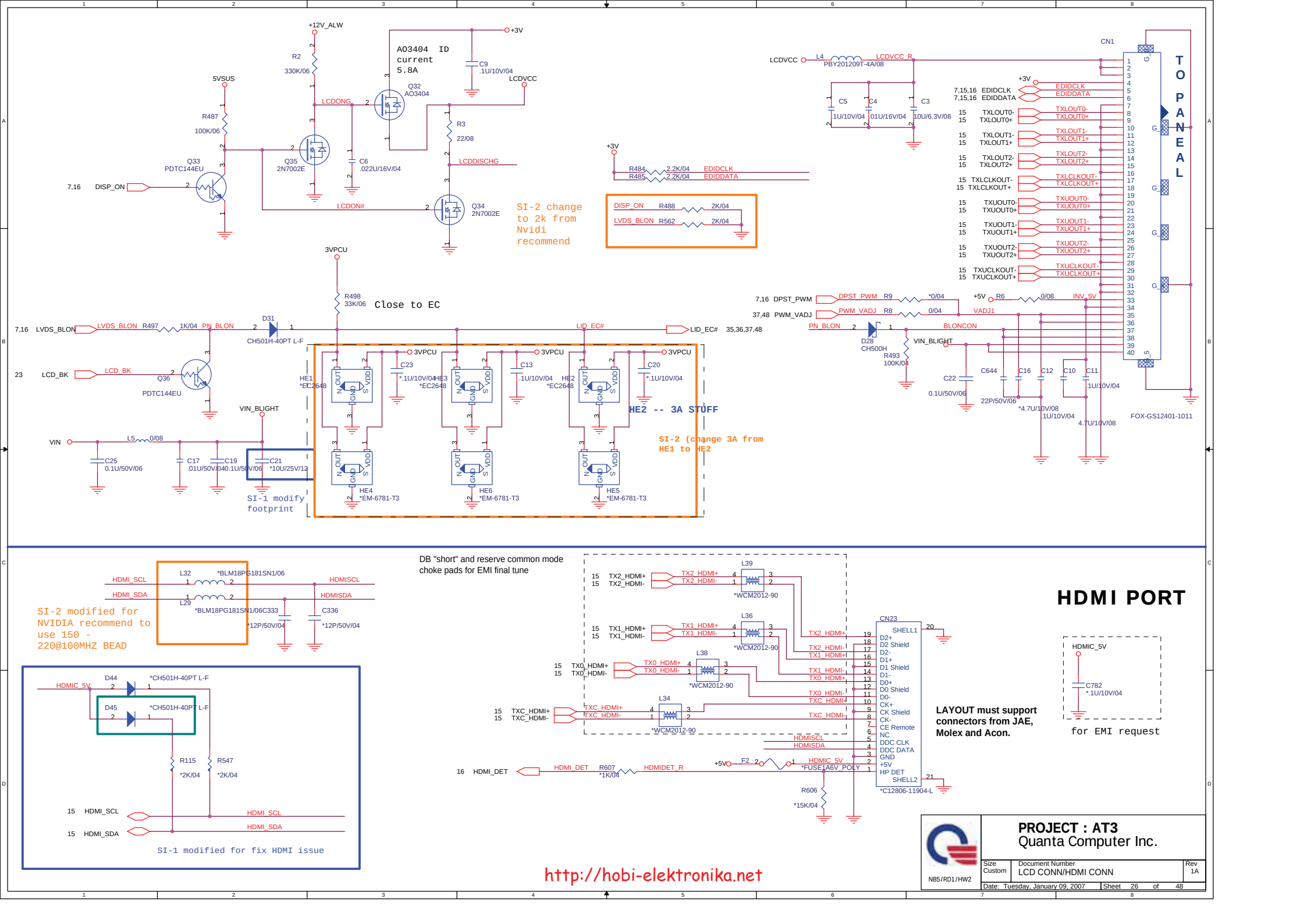
http://hobi-elektronika.net

NB5/RD1/HW2

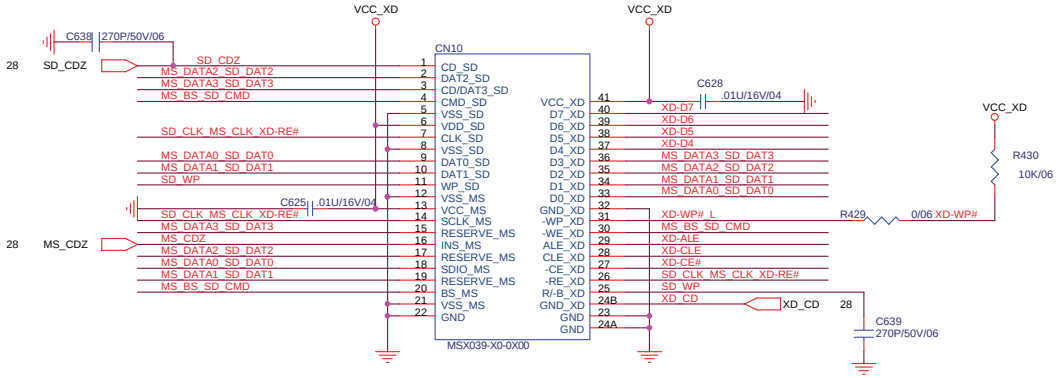
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/TV_OUT	1A

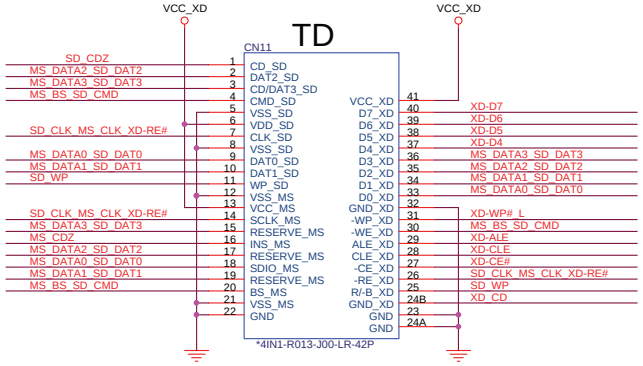
Date: Tuesday, January 09, 2007 Sheet 25 of 48


AO3404 ID current 5.8A
SI-2 change to 2k from Nvidi recommend
Close to EC
HE2 -- 3A STUFF
SI-2 (change 3A from HE1 to HE2
SI-1 modify footprint
TO PANEL
FOX-GS12401-1011
SI-2 modified for NVIDIA recommend to use 150 - 220@100MHZ BEAD
SI-1 modified for fix HDMI issue
DB "short" and reserve common mode choke pads for EMI final tune
HDMI PORT
LAYOUT must support connectors from JAE, Molex and Acon.
for EMI request
http://hobi-elektronika.net
PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
LCD CONN/HDMI CONN
Tuesday, January 09, 2007

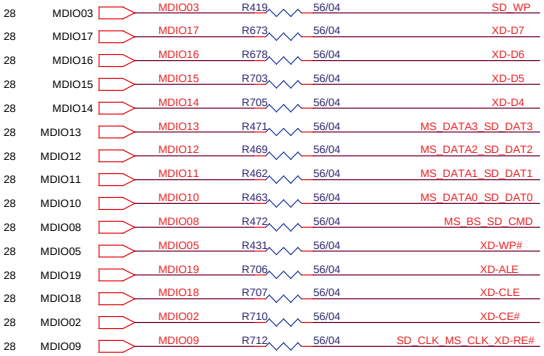
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

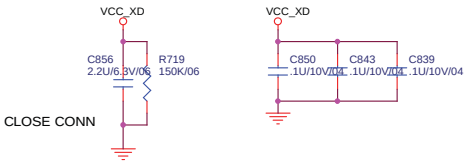


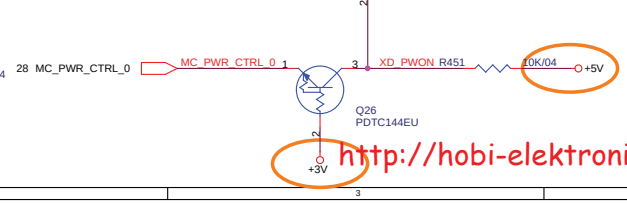
TD



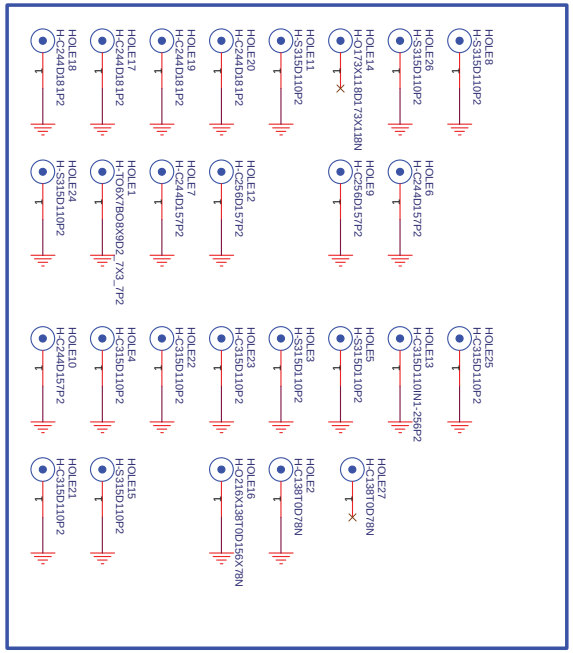
bom create 2'nd source



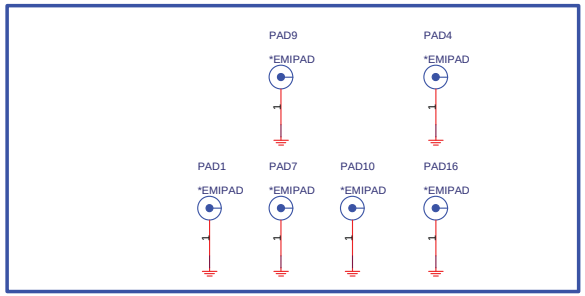




SCREW HOLE

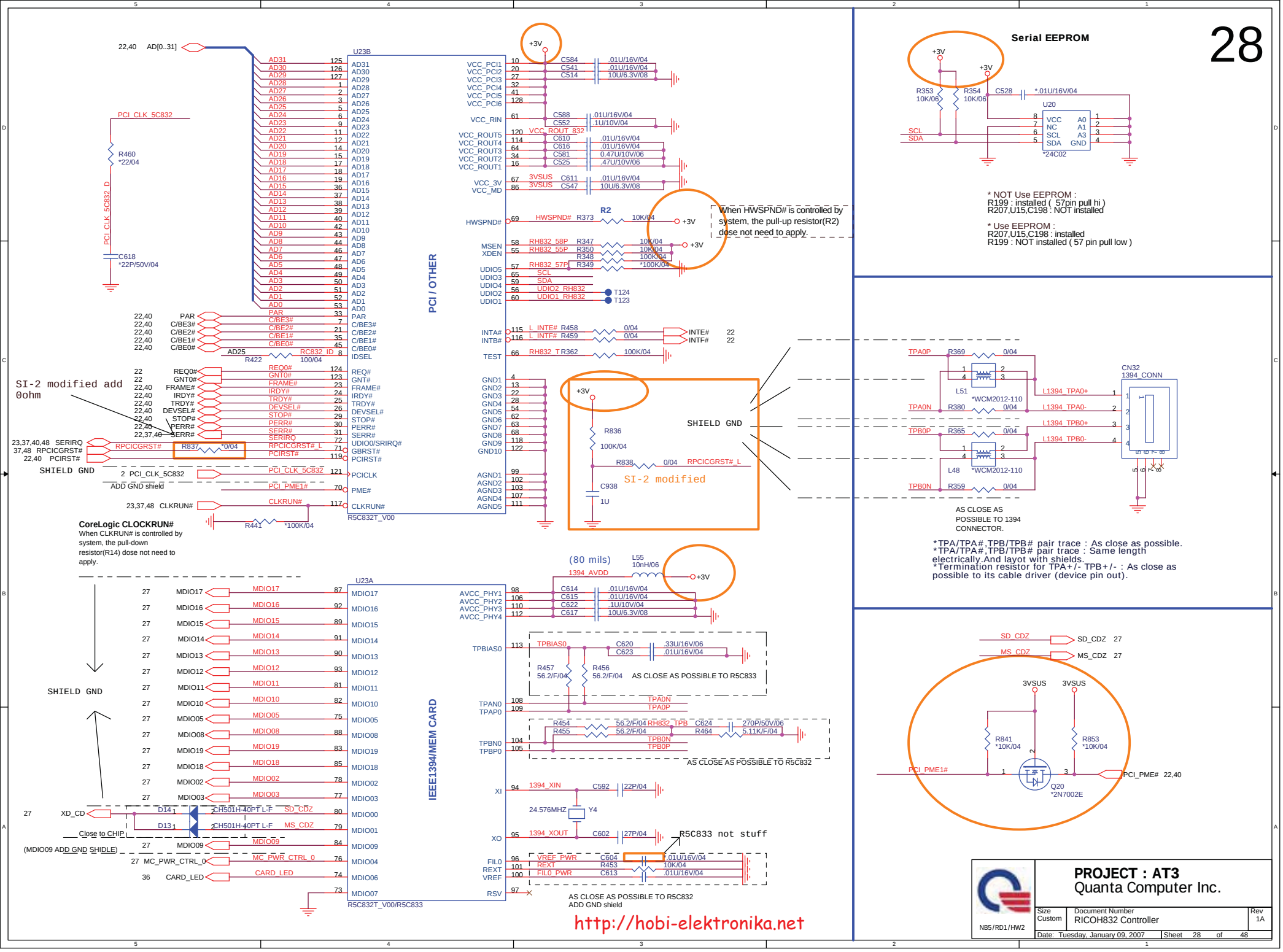


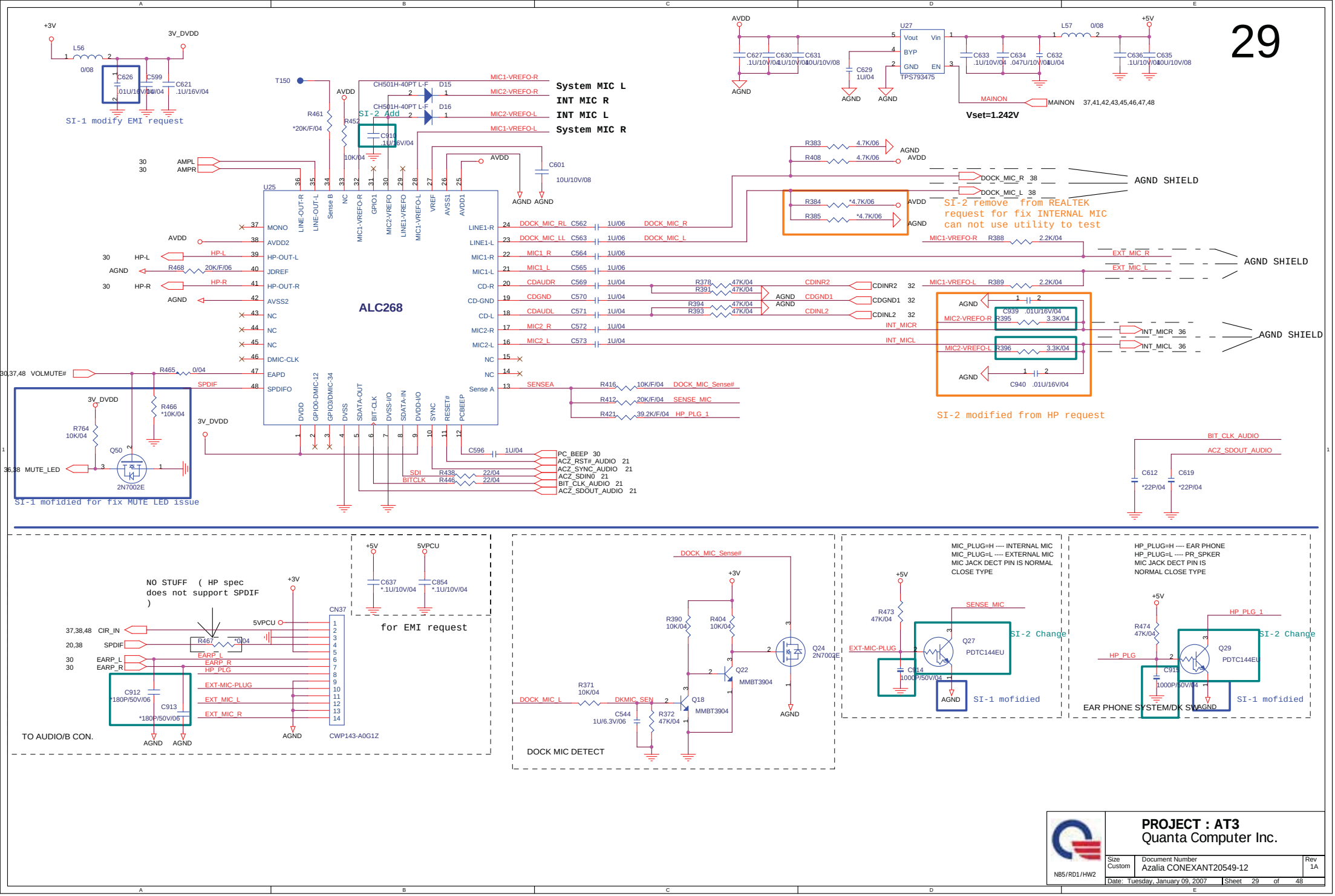
EMI PAD



moden cable sprig

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.		
	Size: Custom	Document Number: CARD READER/HOLE	Rev: 1A
	Date: Tuesday, January 09, 2007	Sheet 27 of 48	





PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 29 of 48

AUDIO AMPLIFIER

INT. SPEAKER

SI-2 remove r739 ,r731 from realtek request for fix BO voice when audio jack unplug

SI-1 ADD EMI request

SI-1 DEL EMI request

SI-1 DEL EMI request

SI-1 ADD EMI request

0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

TPA0312 PWP24

PCSPK BEEP

TO CODE

TO AMP

SI-1 add R765 and remove * part

SI-1 add R807 and remove *part

(AMP BEEP ENABLE AT SYSTEM BOOT)
H=ENABLE
L=DISABLE

LINE OUT Amplifier

LINE OUT Amplifier

MAX4411 EP can NOT be connected to GND. Please leave EP pins floating.

SI-2 modified from HP recommend

QFN20-4X4-5-25P

PROJECT : AT3
Quanta Computer Inc.

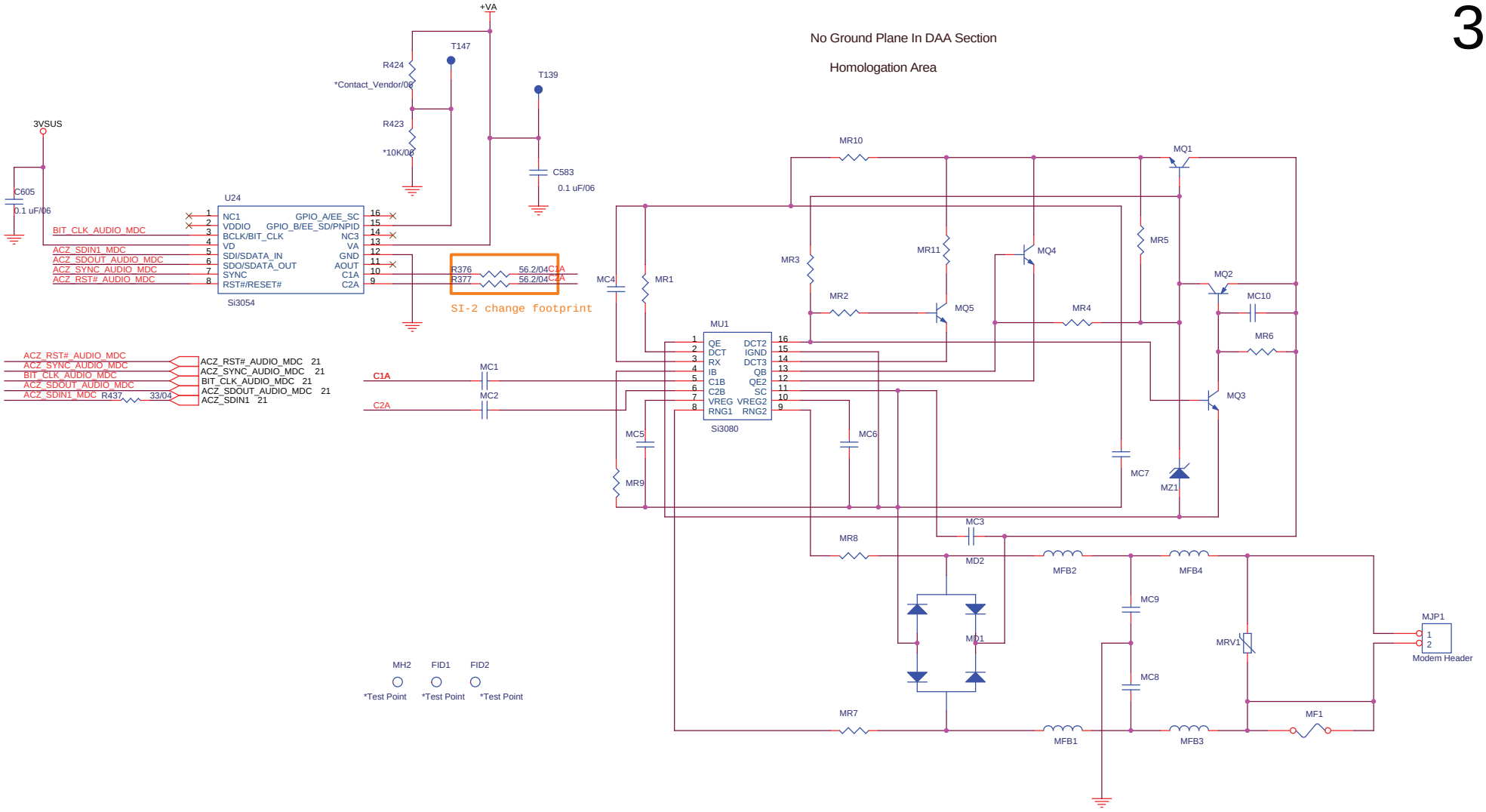
Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 | Sheet 30 of 48

No Ground Plane In DAA Section

Homologation Area

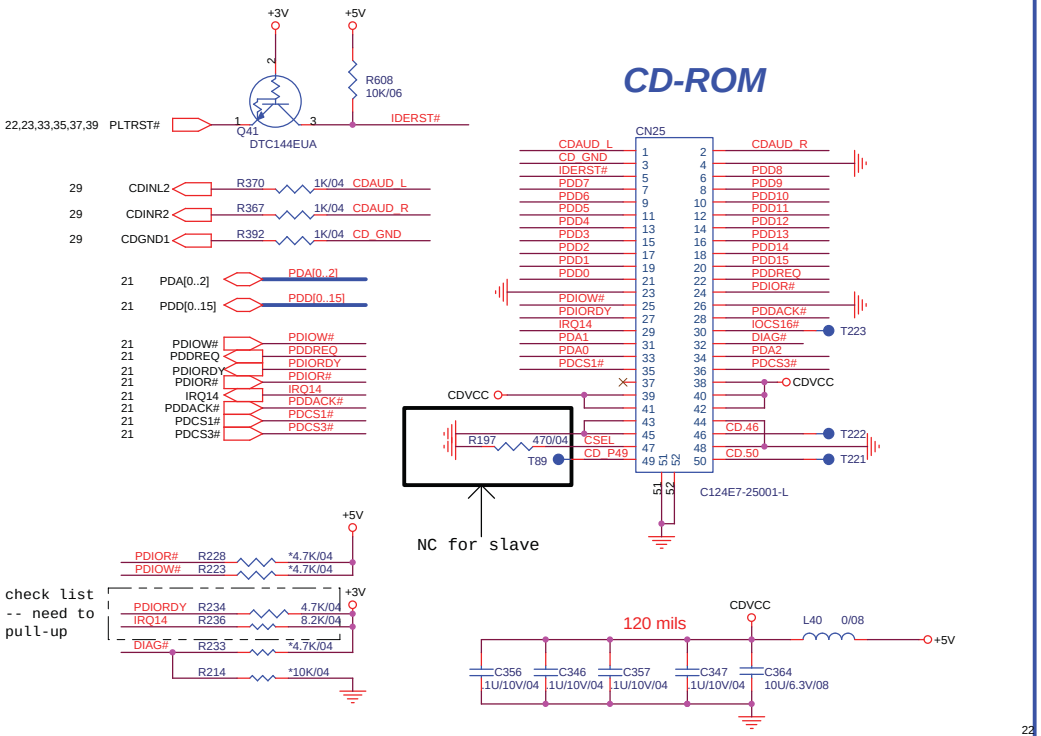


DESIGN SUBJECT TO CHANGE

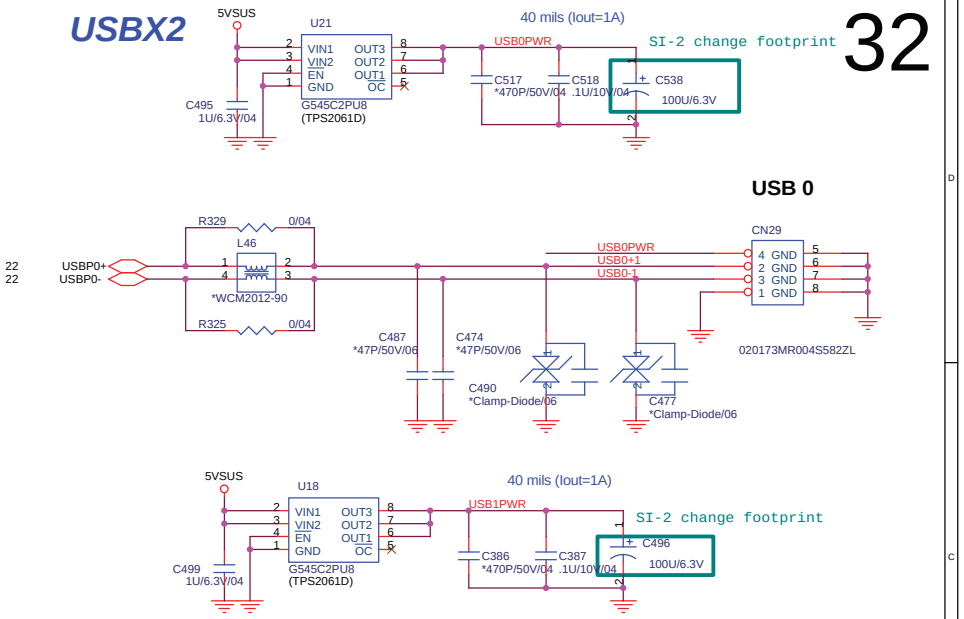
SILICON LABORATORIES CONFIDENTIAL

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom	Document Number: MODEM(DAA) — Rev: 1A
	Date: Tuesday, January 09, 2007	Sheet 31 of 48

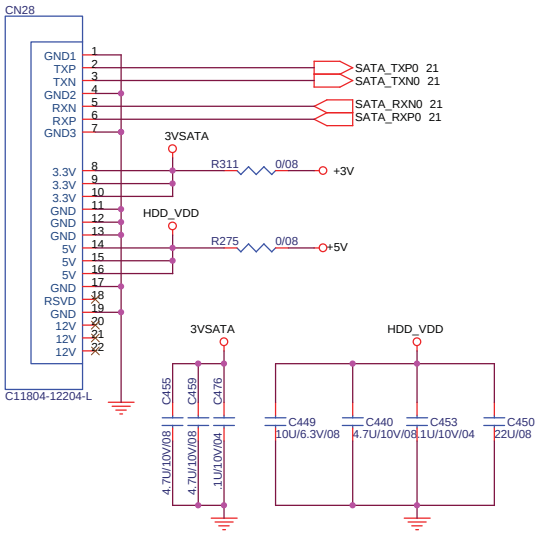
CD-ROM



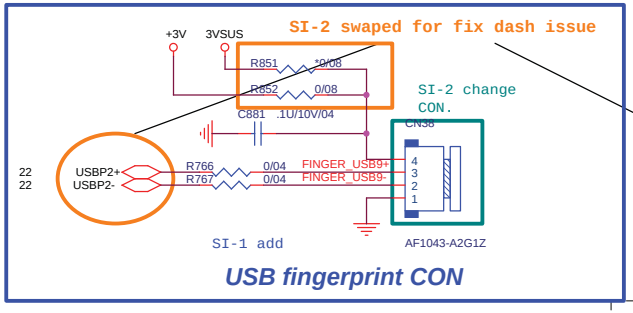
USBX2



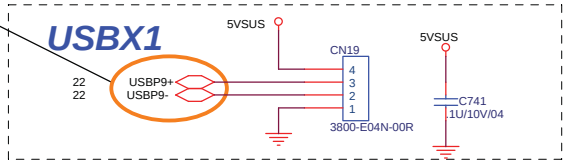
SATA_1 CONNECTOR



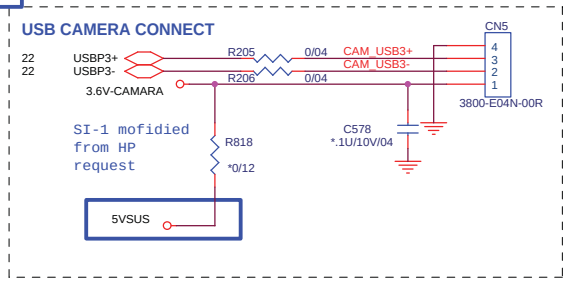
USB fingerprint CON

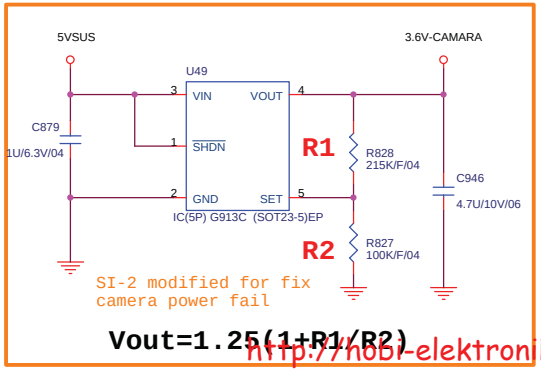


USBX1



USB CAMERA CONNECT





NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A

Date: Tuesday, January 09, 2007 Sheet 32 of 48

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

SI-1 BOM add to fix 10/100 LAN LED issue

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

for 93C56 used. NC if 93C46 is used.

BLOCK A is only for RTL8101E application.

Block A

RJ45

SI-1 modified to fix giga LAN LED issue

Remove R70 for 8111B and 8111C

NS892403:GIGABIT
NS892405:10/100

close U6

PROJECT : AT3
Quanta Computer Inc.

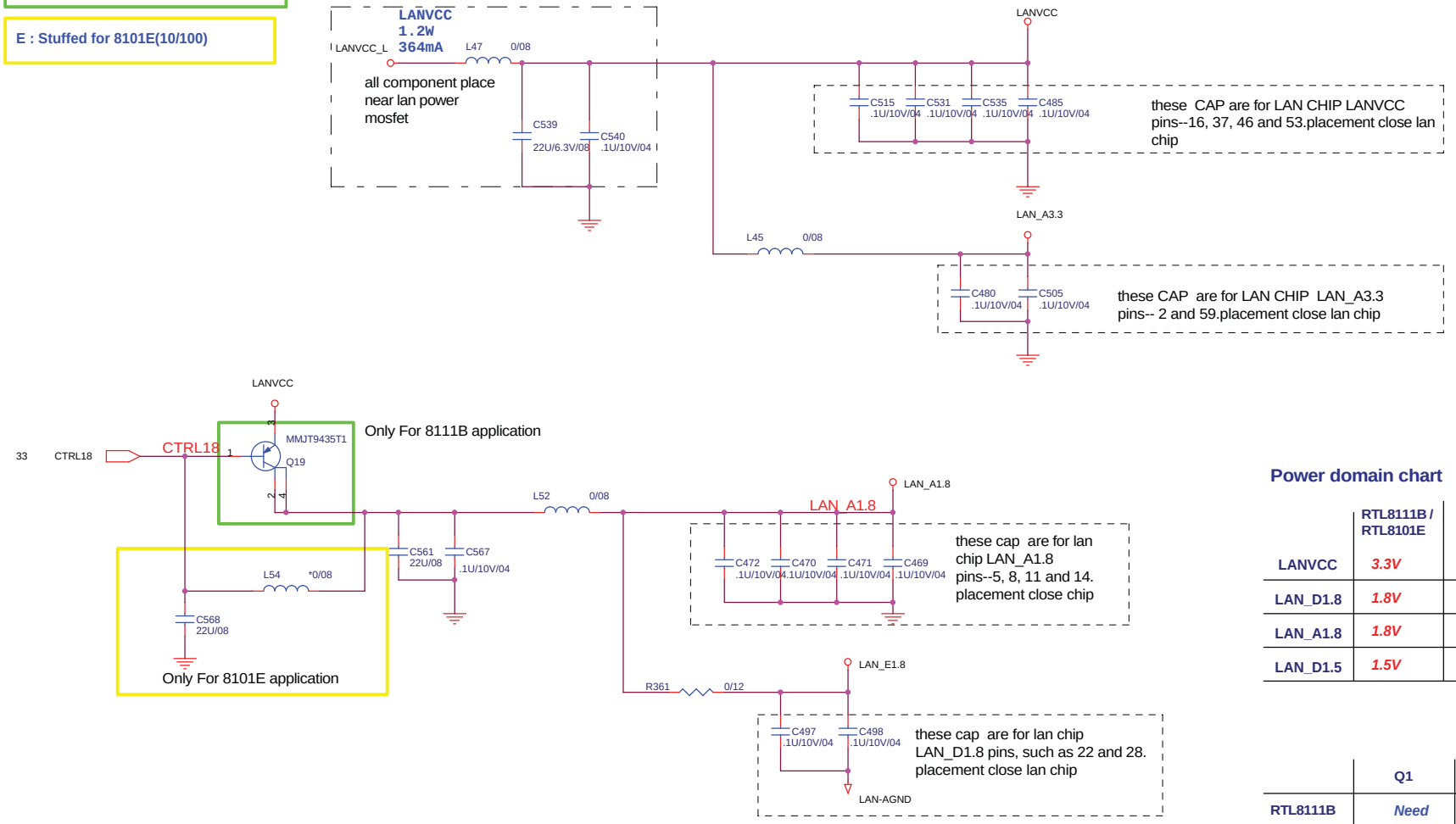
Size	Document Number	Rev
Custom	RTL8111B/8111C/8101E	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 33 of 48

T : Stuffed for RTL8111B(10/100/1000)

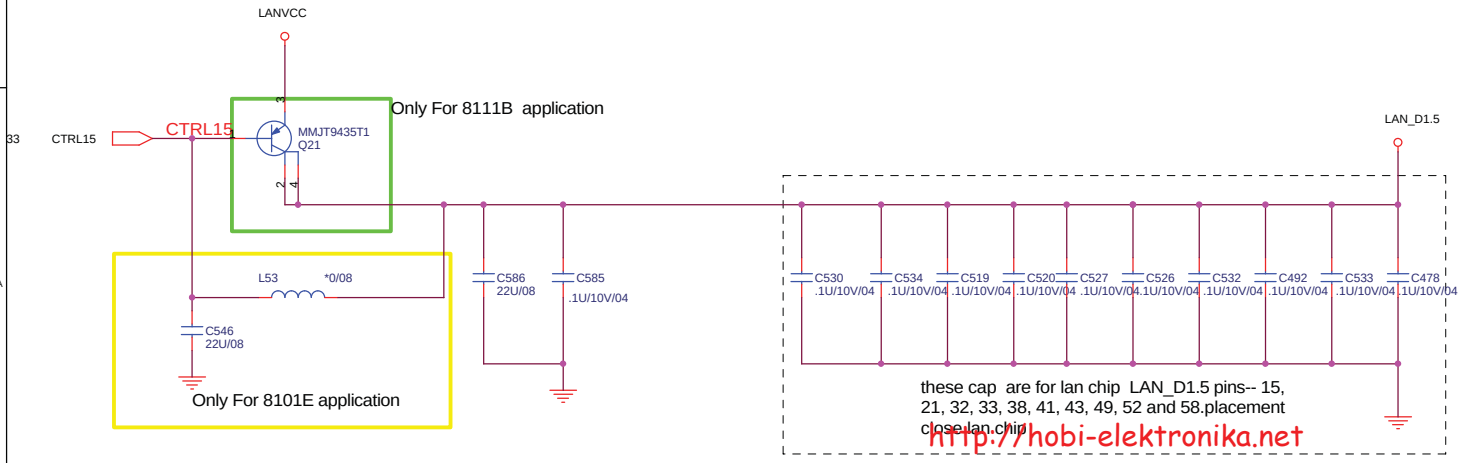
E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E	
LANVCC	3.3V	
LAN_D1.8	1.8V	
LAN_A1.8	1.8V	
LAN_D1.5	1.5V	

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

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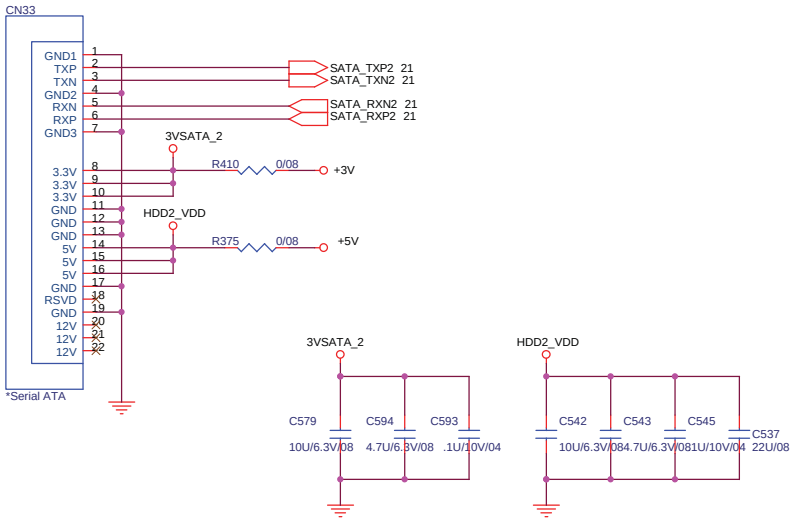
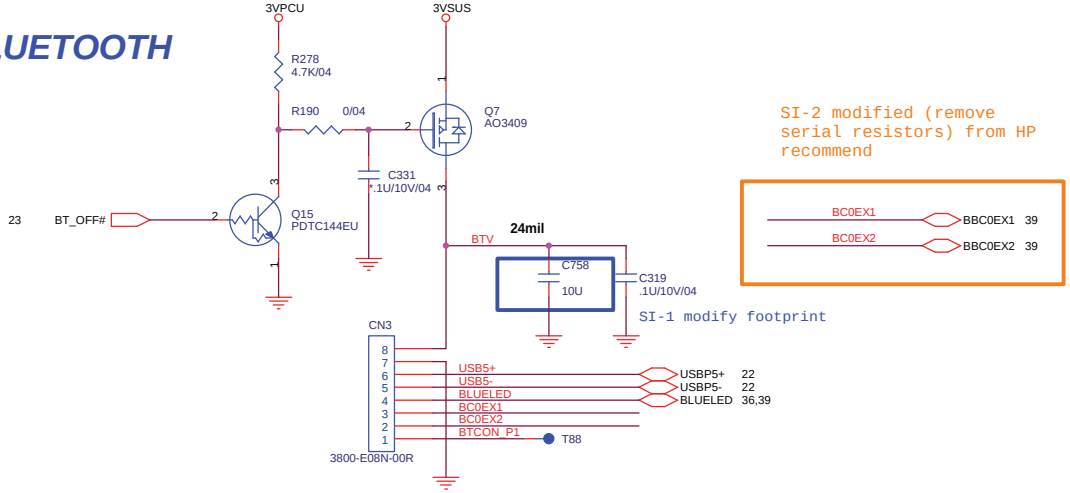
SATA_2 CONNECTOR
For 17"W Second HDD



BLUETOOTH



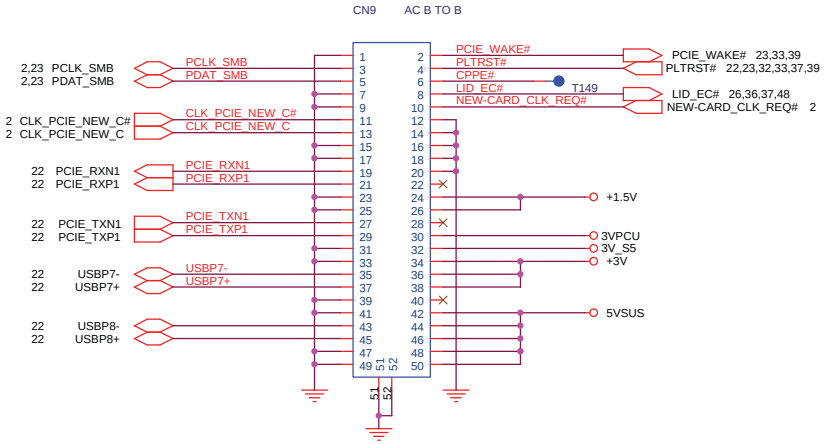
SI-2 modified (remove serial resistors) from HP recommend

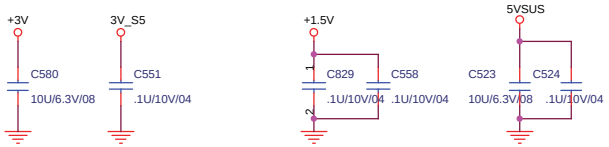
BC0EX1 → BBC0EX1 39

BC0EX2 → BBC0EX2 39

SI-1 modify footprint

NEWCARD





NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	1A

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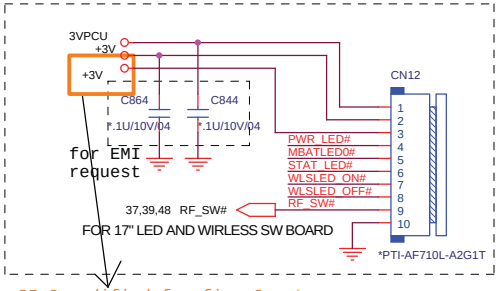
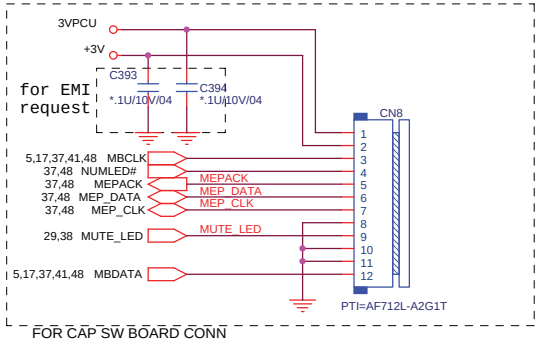
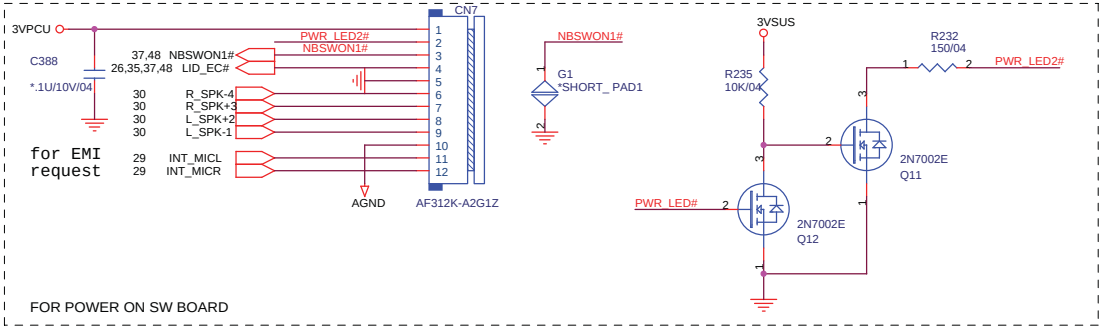
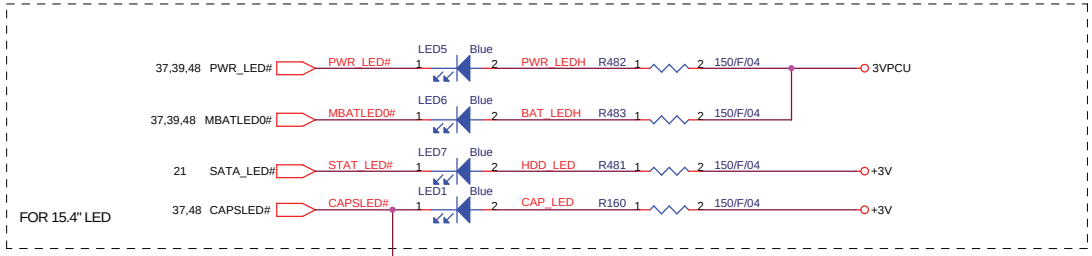
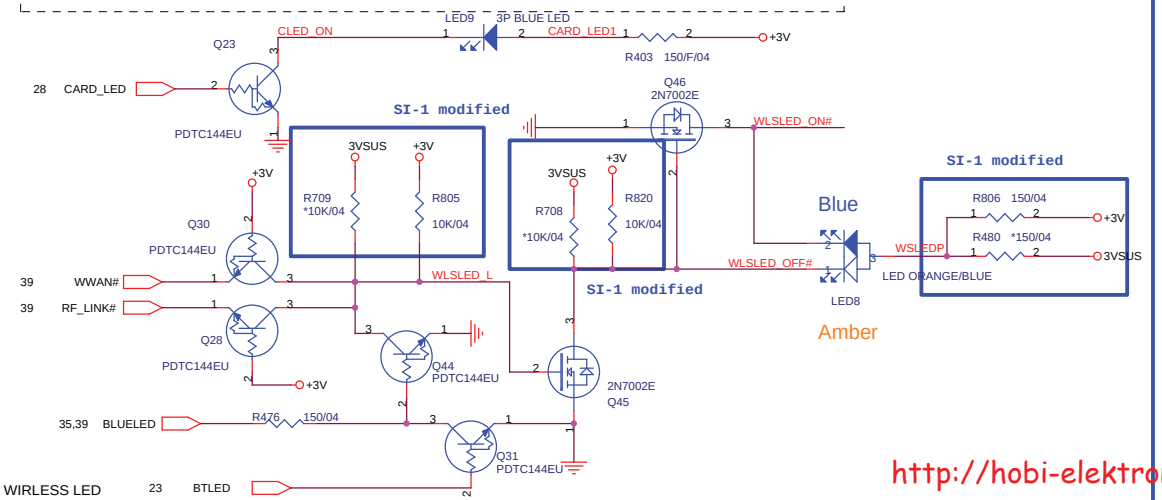


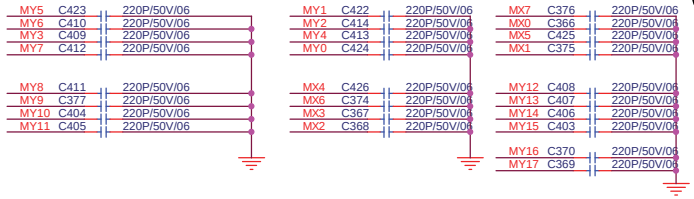
SI-2 modified for fix s3 not support wirless LED



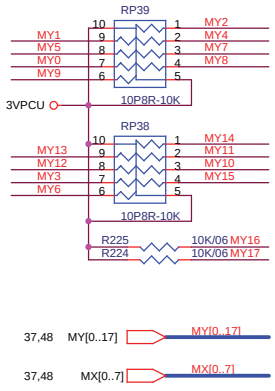


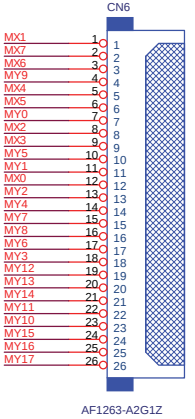


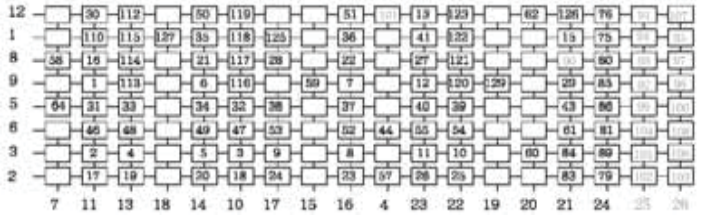




KEYBOARD PULL-UP







NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size: Custom
Document Number: LED/KEYBOARD/SW
Rev: 1A
Date: Tuesday, January 09, 2007
Sheet 36 of 48

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

SI-1 DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified remove ISA BIOS

TOUCH PAD CONNECTOR

25 mils

FOR 15.4"

FOR 17"

SI-1 modify (remove R245 and add R241)

SI-1 modify

SI-2 modified remove ISA BIOS

SI-2 modified remove ISA BIOS

SI-1 ADD

ICH8 has internal pull-up

1M byte SPI BIOS

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size: Custom | Document Number: KB3920/ROM/TP | Rev: 1A

Date: Tuesday, January 09, 2007 | Sheet 37 of 48

CABLE DOCK

support 6A 200mils
CX000480005

SI-1 mofidied (BOM add for support docking SPIDF

+1.5V R522 33/04 C883 .1U/10V/04 SPDDK_V Q37 MMBT3904
20,29 SPDIF R531 510/F/04 SPDIF_DK 2 R525 510/F/04 C681 68P/50V/04 SPD_DK L68 0/06 SPDIF_DOCK

DOCK_VA L61 FBMJ3216HS480NT/12 VA_P
41 DOCK_VA C658 0.1U/50V/06 C651 0.1U/50V/06

CN18
VA_P 44 VDD 43 VDD 43 VA_P
25 PR_GEN PR_GEN R45 0/04 CRT_GDK
25 PR_RED PR_RED R38 0/04 CRT_RDK
25 DDCDAT2
25 PR_BLU PR_BLU R54 0/04 CRT_BDK
25 PR_HSYNC R811 0/06 PR_HSYNC_D
25 DDCCLK2
SI-1 ADD EMI request
USB4-1
25 PR_VSYNC R812 0/06 PR_VSYNC_D
SI-1 ADD EMI request
USB4+1
33 +LAN_MX3_PR
33 -LAN_MX3_PR
33 +LAN_MX2_PR
33 -LAN_MX2_PR
33 +LAN_MX1_PR
33 -LAN_MX1_PR
33 +LAN_MX0_PR
33 -LAN_MX0_PR
VIN C894 0.1U/50V/06
42 VSS 46 VSS 45 41 45
QL1122L-H212AR-7F
SI-1 ADD EMI request
37 S-YD-DO-PR R510 0/04 S-YD-DO 25
35 S-CD-DO-PR R516 0/04 S-CD-DO 25
33 S-CVBS-DO-PR R518 0/04 S-CVBS-DO 25
31
29 CIR_IN 29,37,48
27 PWR_ON
25 MUTE_LED MUTE_LED 29,36
23 SLP_BTN# SLP_BTN# 37
21 JACK_DETECT# JACK_DETECT# 30
19 VOLME_UP# VOLME_UP# 37,48
17 VOLME_DN# VOLME_DN# 37,48
15 SPDIF_DOCK
13 AGND
11 RSPK_DK C60 100U/6.3V DOCK_RSPK+ 30
9 LSPK_DK C75 100U/6.3V DOCK_LSPK+ 30
7
5 DOCK_MIC_R 29
3 DOCK_MIC_L 29
1 DOCK_PRESENT AGND

22 USBP4- R528 0/04 USB4-1
22 USBP4+ L67 *CMM211T-900M-S R526 0/04 USB4+1

+3V R844 100K/04 3VPCU R548 *100K/04 PR_INSERT# PR_INSERT# 25
docking insert is HI voltage
DOCK_PRESENT R579 1K/04 DKPR# Q40 2N7002E R573 2K/F/06

PR_HSYNC_D
PR_VSYNC_D
C892 *47P/50V/06 C893 *47P/50V/06
SI-1 ADD EMI request

+5V D33 SW1010CPT SW1010CPT D34
5VSUS R520 10K/04 DK_PWRON PWR_ON R527 15K/04
S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

DOCK_MIC_R
DOCK_MIC_L
RSPK_DK
LSPK_DK
JACK_DETECT#
VOLME_DN#
CIR_IN
C673 *120P/50V/04 C677 *120P/50V/04 C674 270P/25V/04 C897 C898 C902 C903 180P/50V/04
SI-1 ADD EMI request

PR_GEN
PR_RED
PR_BLU
CRT_GDK
CRT_RDK
CRT_BDK
C918 C919 C920 5.6P/06
C941 C942 C943 5.6P/06
PR_GEN
PR_RED
PR_BLU
R56 R30 R39 150/F/04
SI-2 modified for fix docking R.G.B signals measure fail

S-YD-DO-PR
S-CD-DO-PR
S-CVBS-DO-PR
R519 R517 R506 *150/F/04

FAN

EXTERNAL VGA FAN RESEVRE
+5V L72 *0/08 20 mil 37,48 FAN2ON 5VFAN2 CN20
C739 *2.2U/6.3V/06 C740 .1U/10V/04
*PTI=CWP043-A0G1T
near to connector.
FAN2 PWM CONNECTOR

CPU FAN
D39 *SSM34PT L-F CN22
+5V L73 0/08 20 mil 37,48 FAN1ON 5VFAN1
C749 2.2U/6.3V/06 C748 1U/10V/04
PTI=CWP043-A0G1T
+5V R594 4.7K/06 FAN1SIG FAN1SIG 37,48
FAN1 PWM CONNECTOR

PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom | Document Number CABLE DOCKING/FAN | Rev 1A
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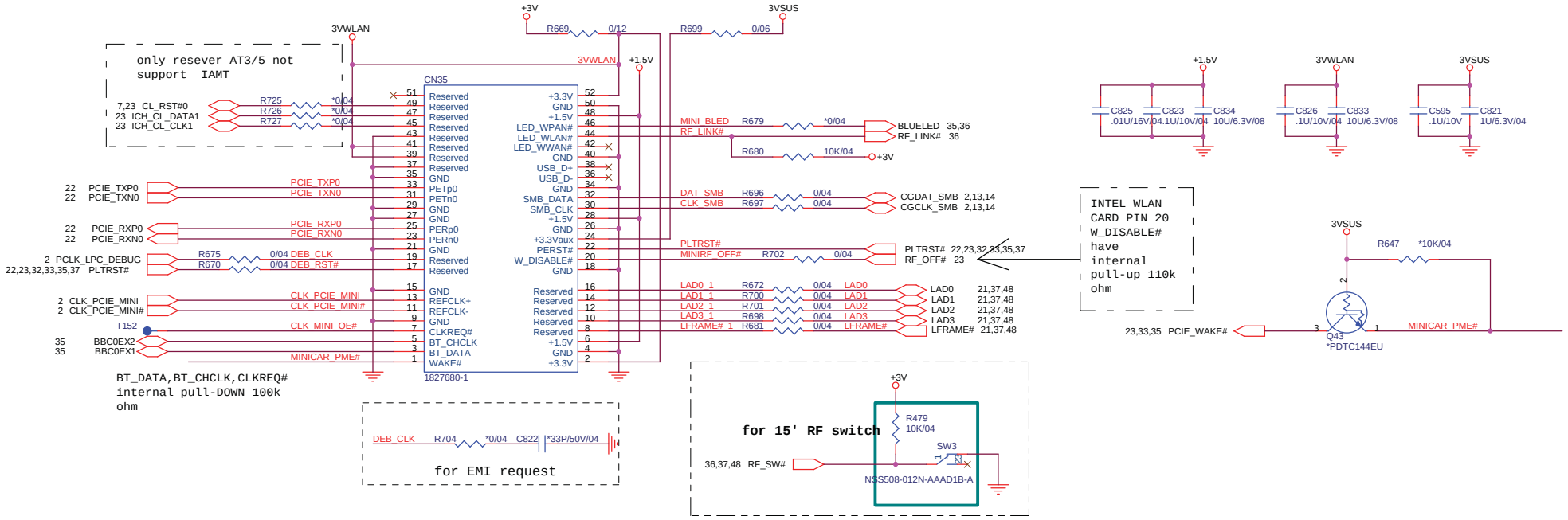
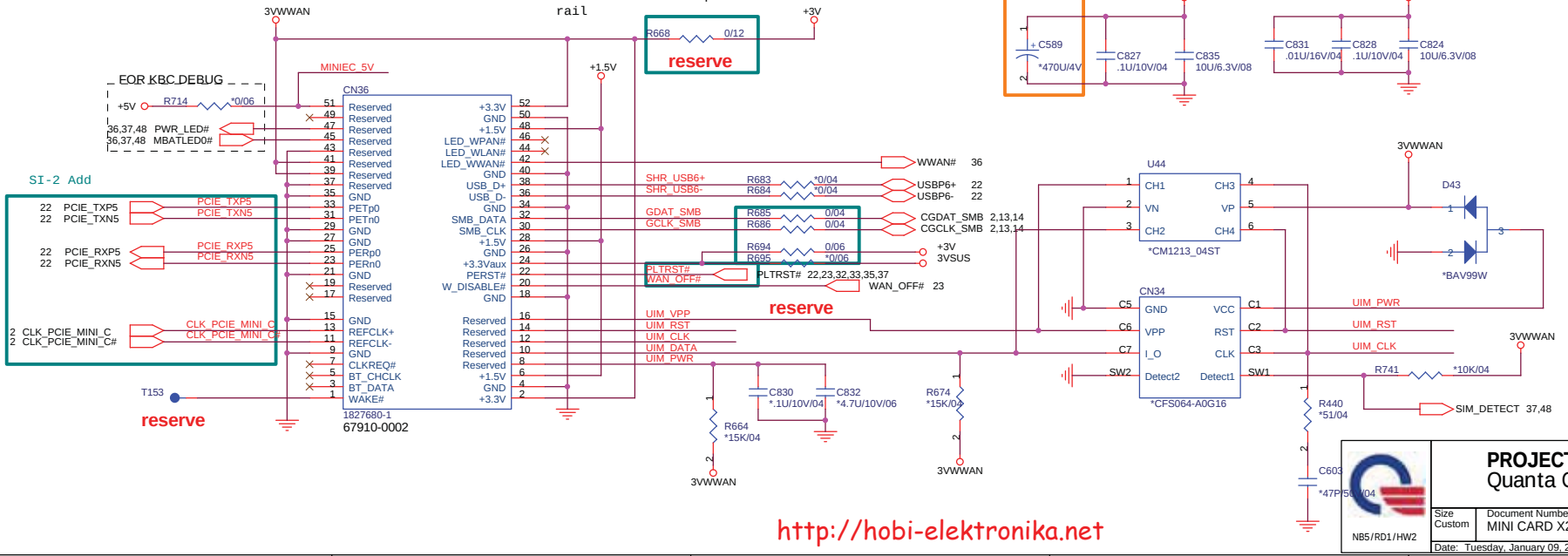
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

SI-2 modified
(BOM remove C589
)



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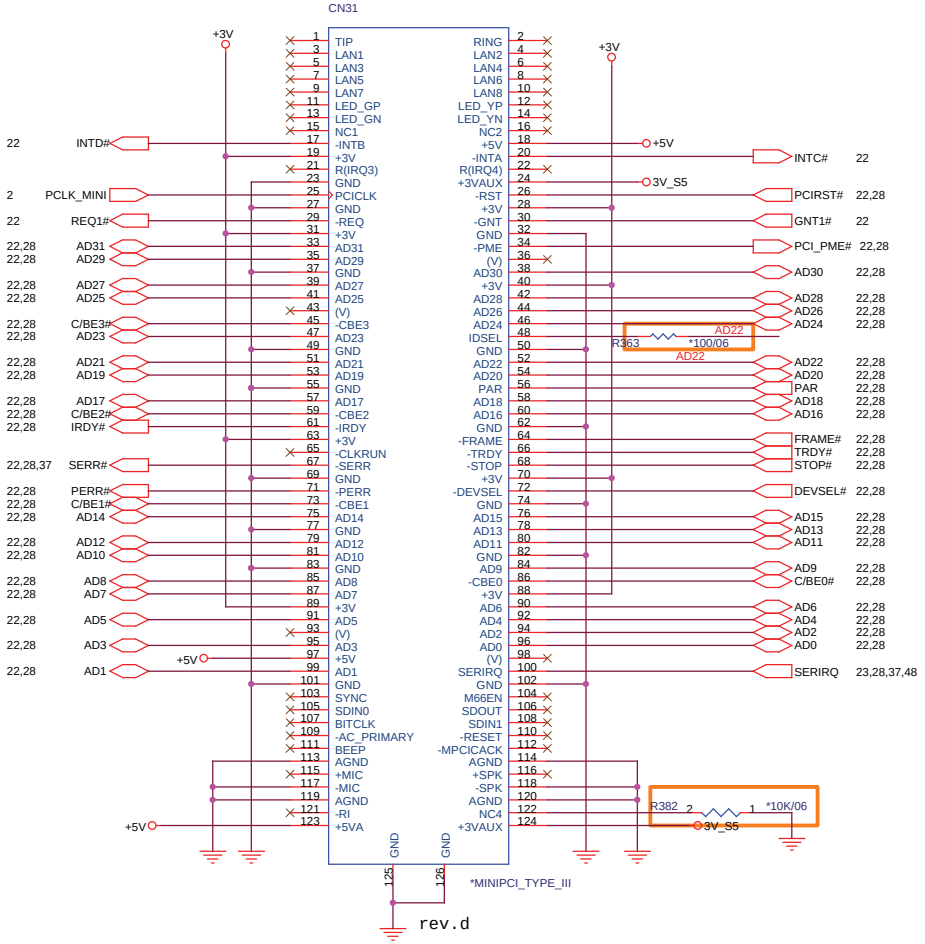
PROJECT : AT3 Quanta Computer Inc.		
Size: Custom	Document Number: MINI CARD X2	Rev: 1A
NB5/RD1/HW2	Date: Tuesday, January 09, 2007	Sheet 39 of 48

MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



NB5/RD1/HW2	PROJECT : AT3 Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCI TYPE III SLOT	Rev: 1A
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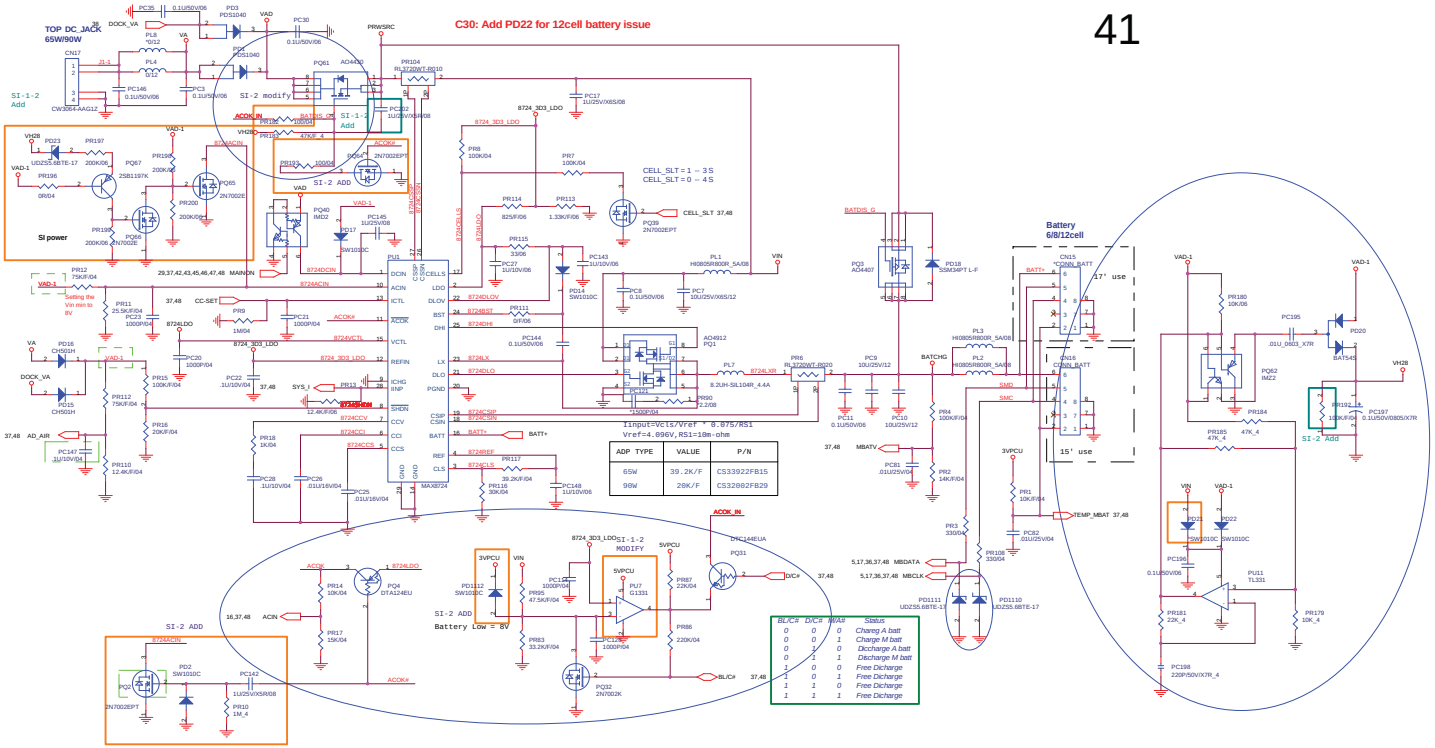

PROJECT : AT3
Quanta Computer Inc.

Size: D	Document Number: SYSTEM CHARGER(MAX8724)	Rev: 1A
Date: Tuesday, January 09, 2007	Sheet 41 of 48	

NB5/RD1/HW2

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Rds(on) 13m ohm

Rds(on) 15m ohm

Max Power Consumption 1.6W

For G73 Only

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PROJECT : AT3 Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom; Document Number: 3v/5v	Rev: 1A
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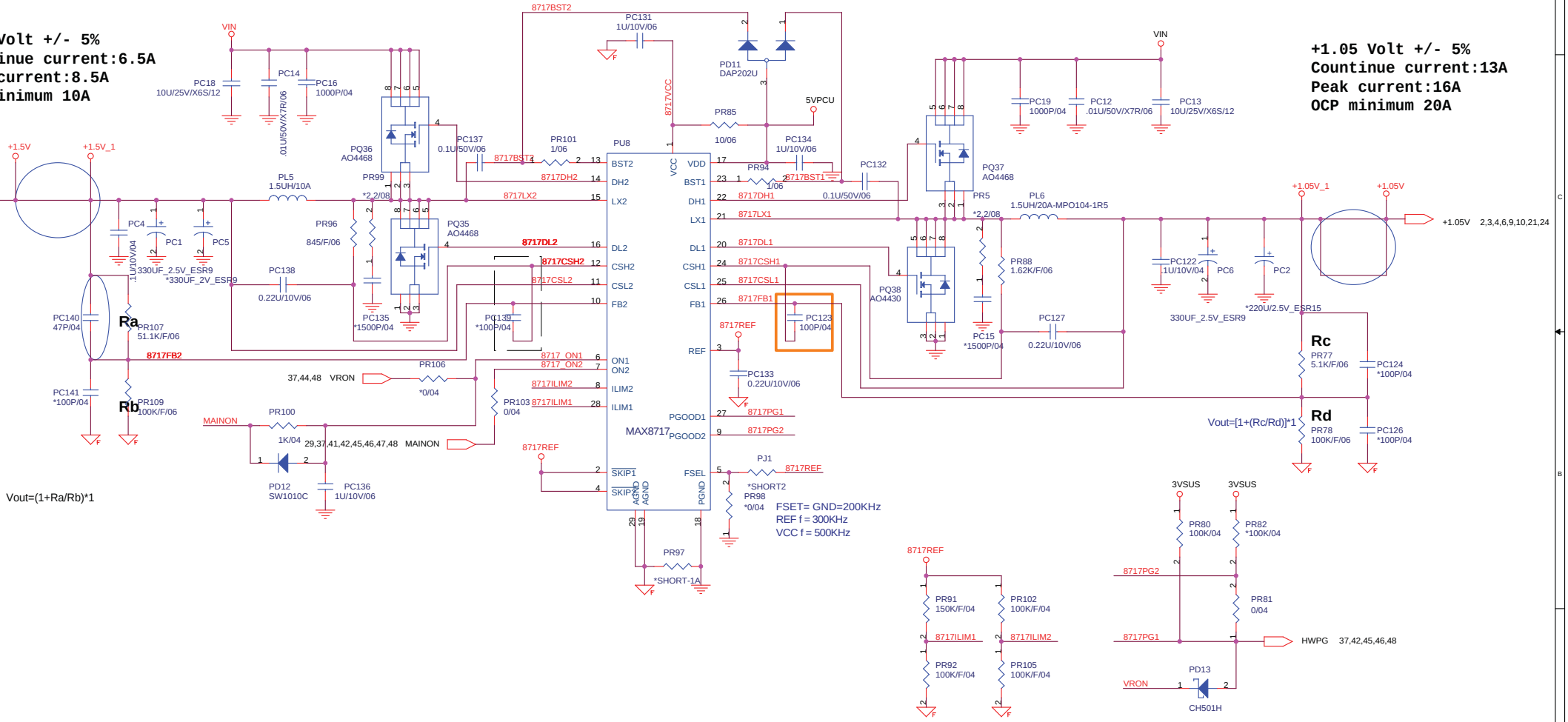
+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



PROJECT : AT3 Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
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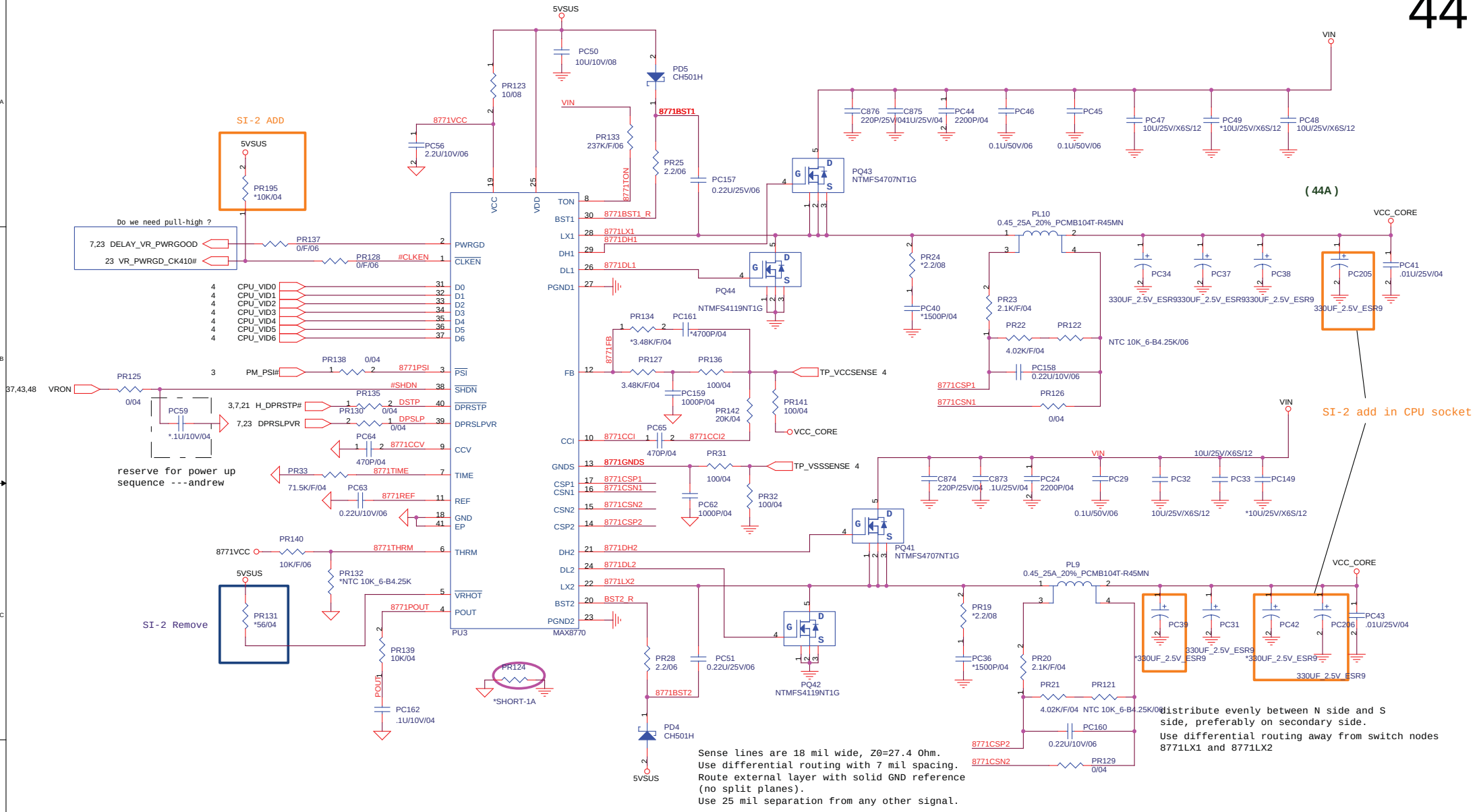

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU_CORE(MAX8771)	1A
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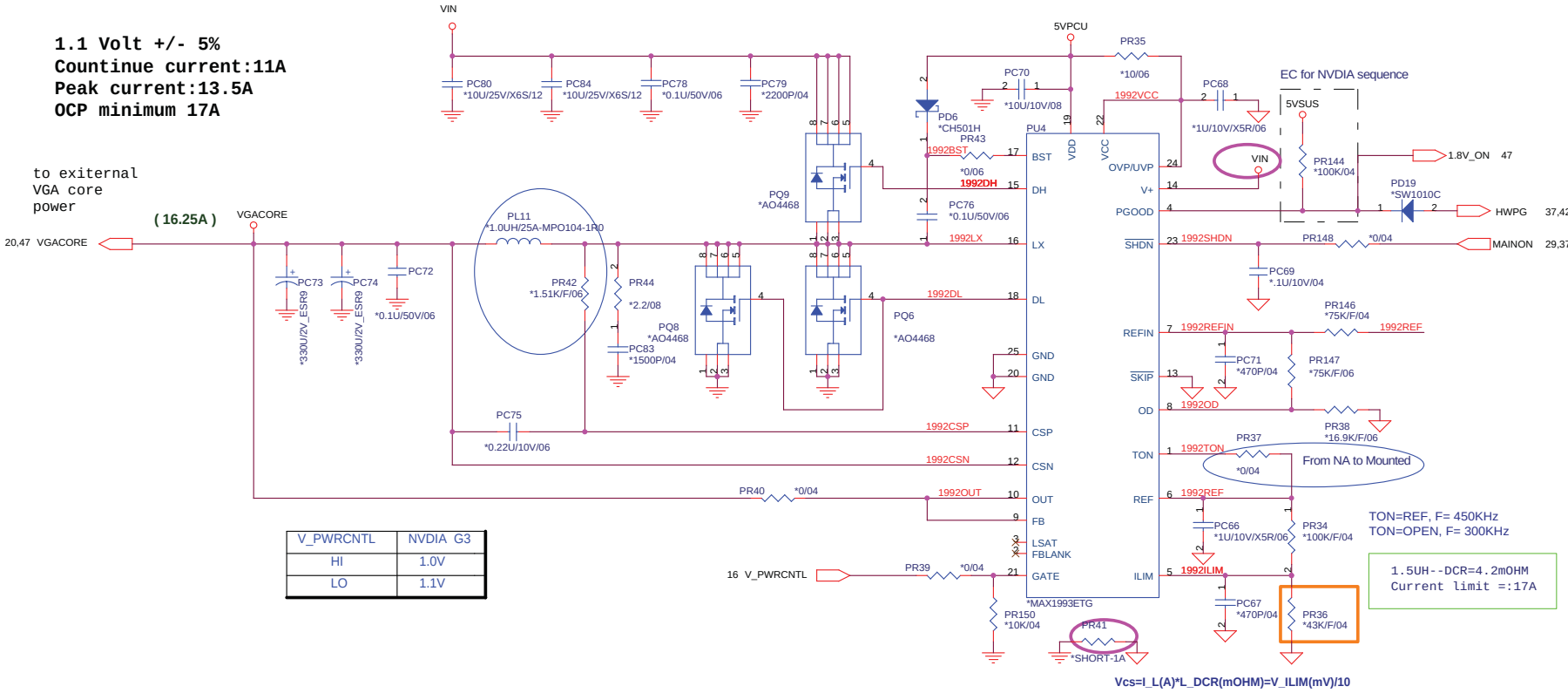
1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A

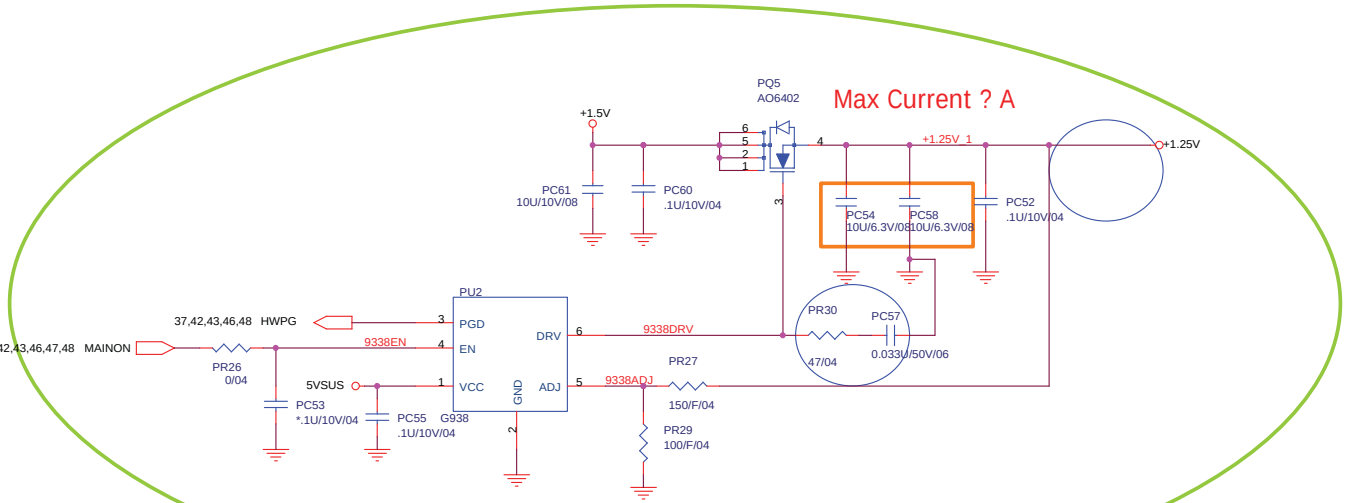
to exiternal
VGA core
power

(16.25A)



V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10



Vout1=(1+R1/R2)*0.5

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGACORE (MAX1993)	1A

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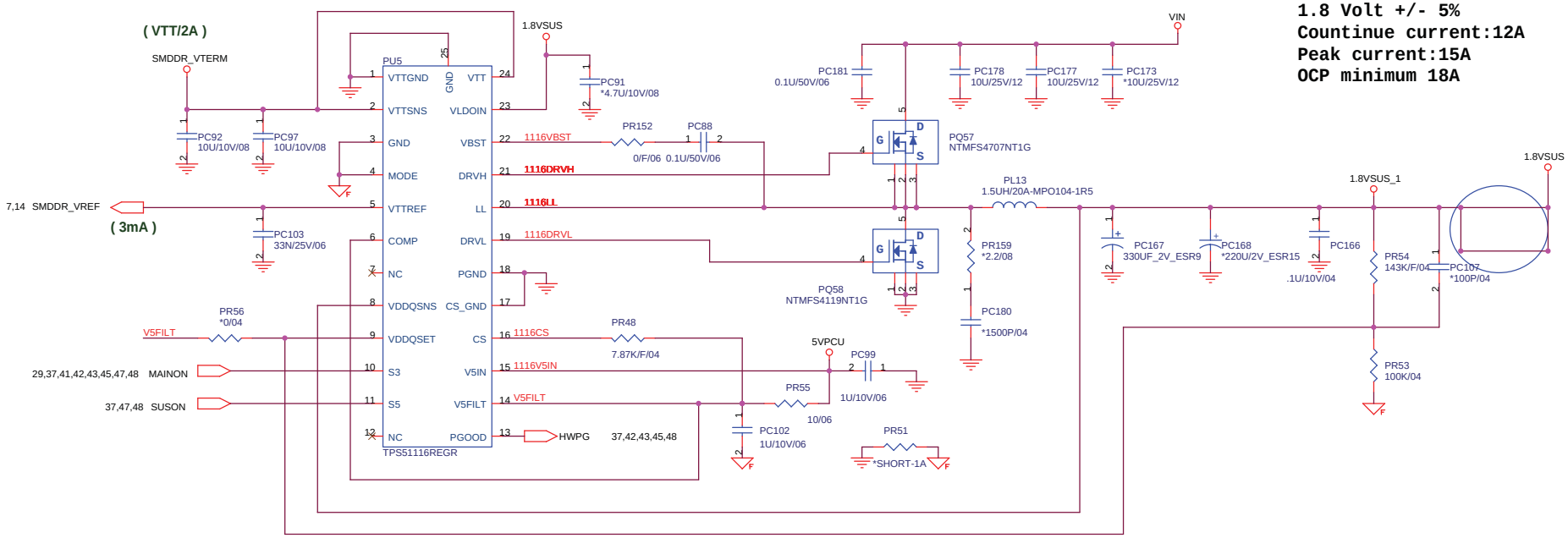

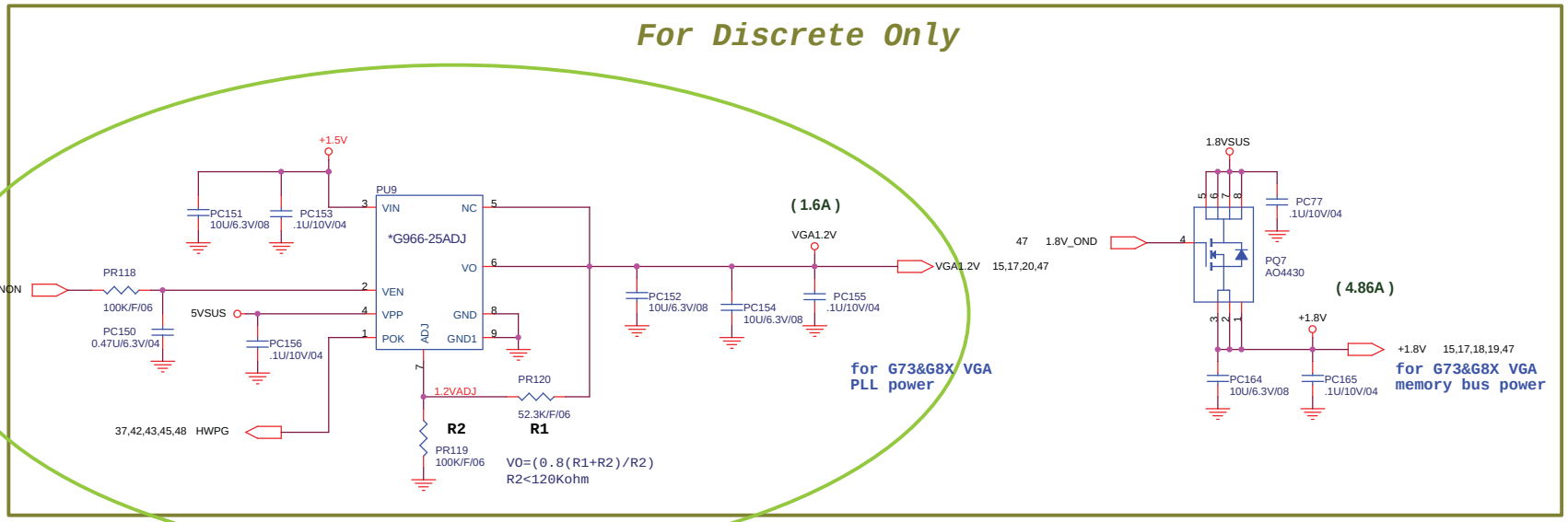

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NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	1A

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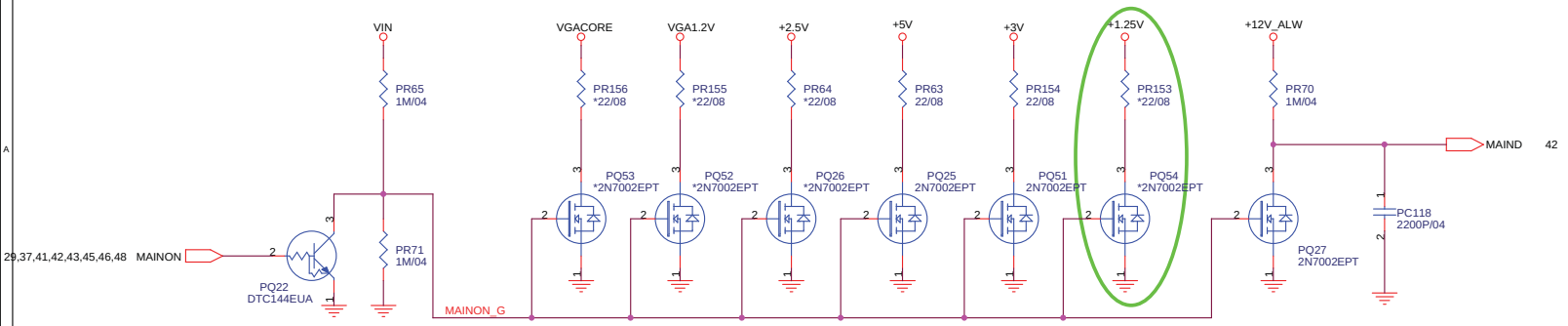
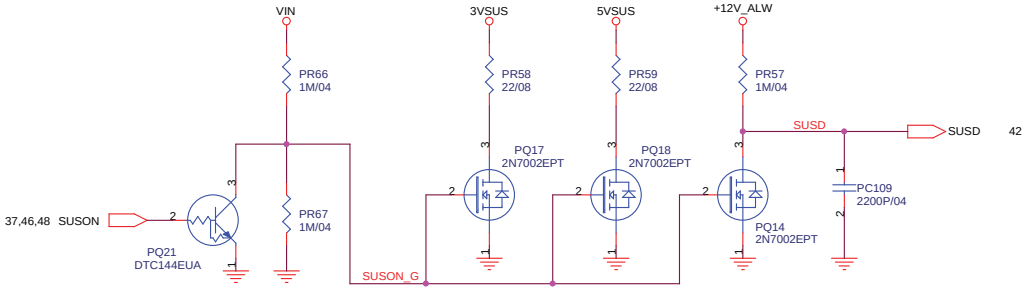
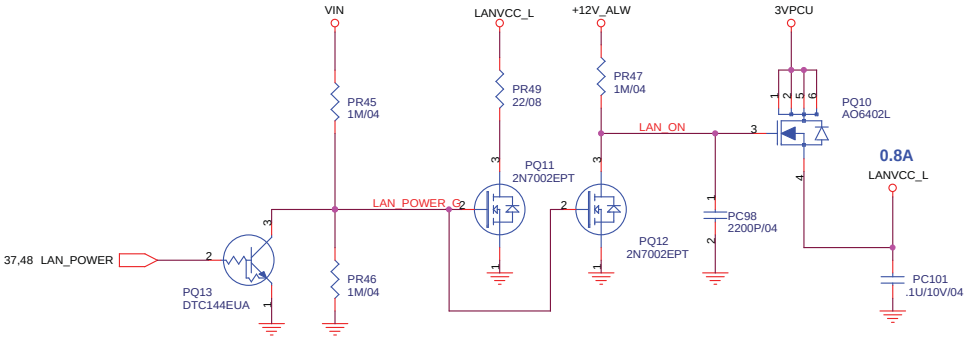
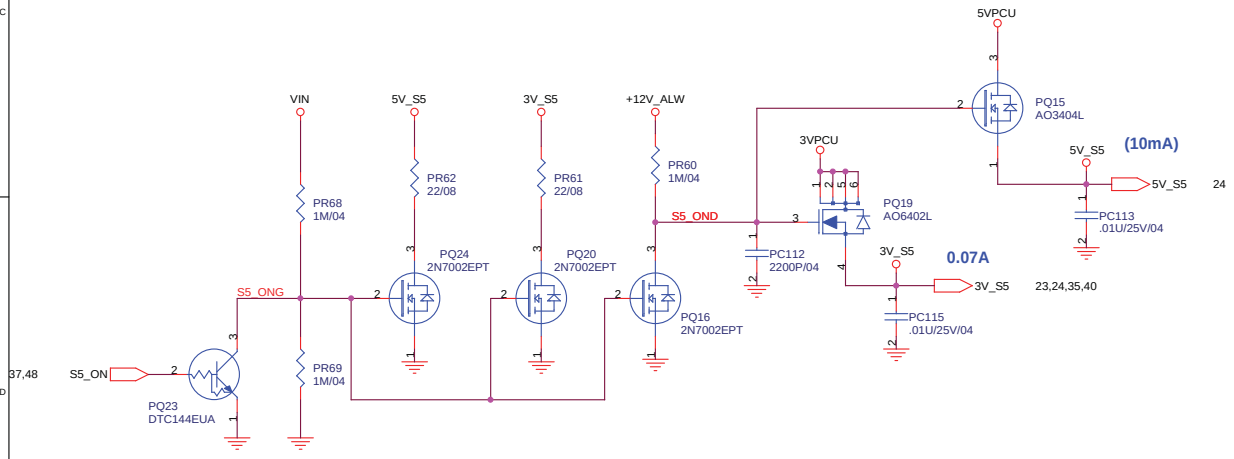
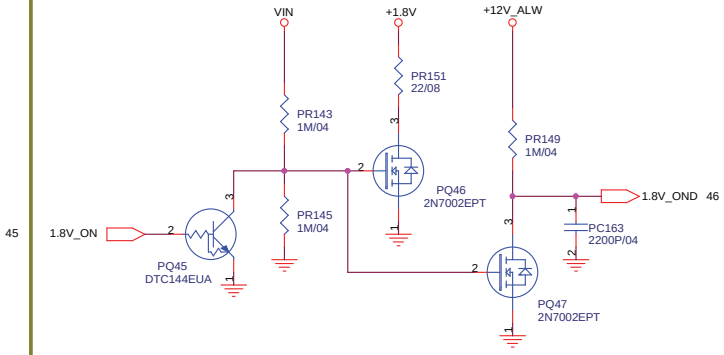








For Discrete Only



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

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Custom	DISCHARGE	1A
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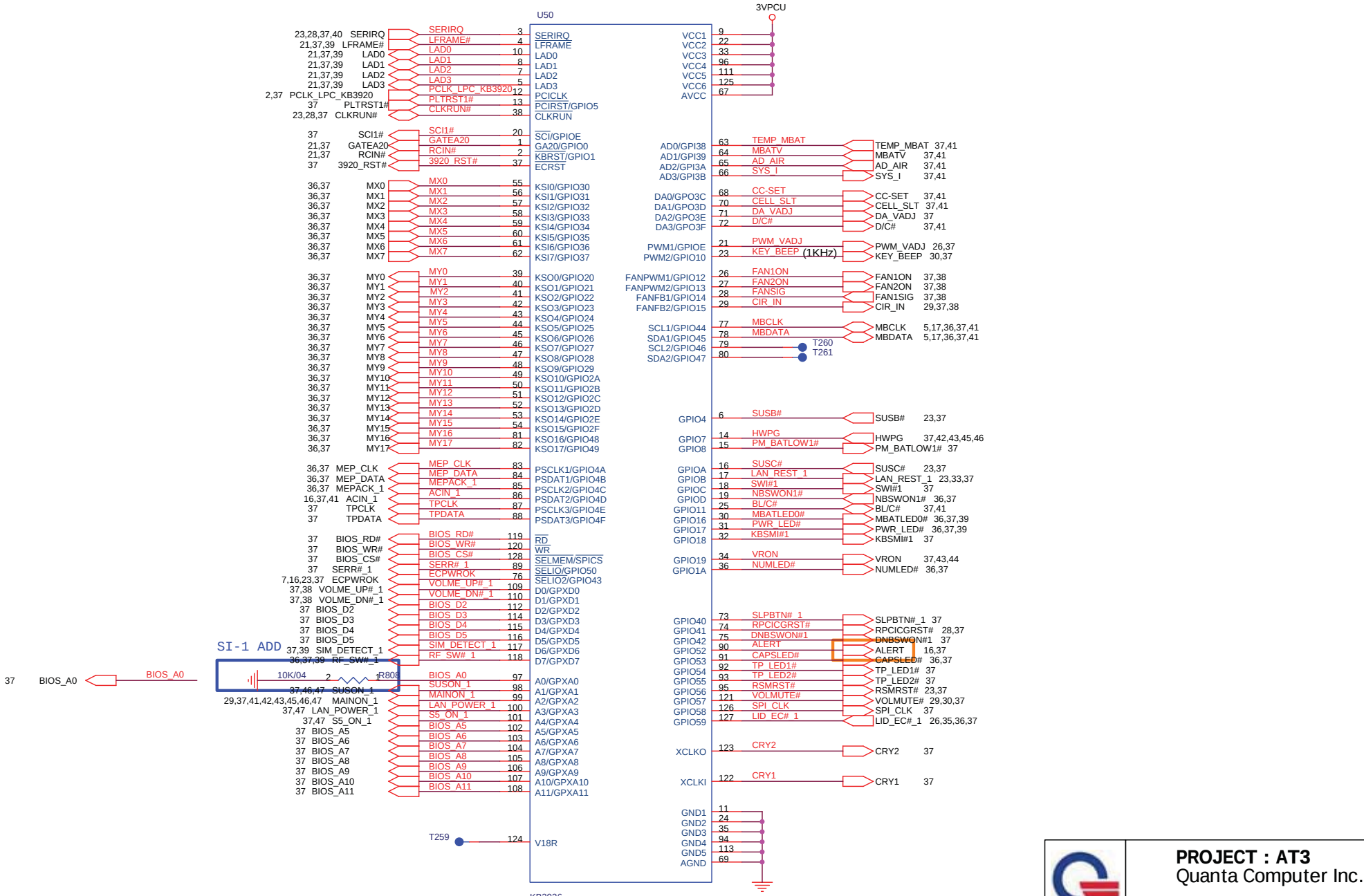

PROJECT : AT3
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NB5/RD1/HW2

Size	Document Number	Rev
B	KB3926	1A
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